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IEEE 802.11a/b/g 무선 랜을 위한 고속 AFC 기법의 CMOS LC VCO의 설계

(Design of CMOS LC VCO with Fast AFC Technique for IEEE 802.11a/b/g Wireless LANs)

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요 약

본 논문에서는 IEEE 802.11a/b/g 무선 랜을 위하여 고속 AFC 기법이 적용된 CMOS LC VCO의 설계를 다룬다. 1.8V 0.18μm CMOS 공정을 사용하였으며, 현재 국제적으로 표준화가 진행된 모든 무선 랜 응용에 적합하도록 인덕터 및 캐패시터를 스위칭하는 방법으로 5.8GHz 대역, 5.2GHz 대역 및 2.4GHz 대역에서 동작하도록 설계하였다. 또한 주파수-전압 특성을 선형화하기 위하여 최적화된 버랙터 바이어싱 기법을 사용하였으며, 필요로 하는 모든 대역에서 저잡음 특성을 유지하기 위하여 4비트 캐패시터 뱅크를 사용하고, 광대역 디지털 주파수 검출기를 이용한 고속 AFC 기법을 구현하여 그 동작을 확인하였다.

Abstract

CMOS LC VCO with fast response adaptive frequency calibration (AFC) technique for IEEE 802.11a/b/g WLANs is designed in 1.8V 0.18μm CMOS process. The possible operation is verified for 5.8GHz band, 5.2GHz band, and 2.4GHz band using the switchable L-C resonators. To linearize its frequency-voltage gain (Kvco), optimized multiple MOS varactor biasing technique is used. In order to operate in each band frequency range with reduced VCO gain, 4-bit digitally controlled switched- capacitor bank is used and a wide-range digital logic quadricorrelator (WDLQ) is implemented for fast frequency detector.

Keywords: CMOS, VCO, AFC, WLAN, WDLQ

I. Introduction

The voltage-controlled oscillator (VCO) with wide tuning features is a major concern in the three different wireless LAN standards (802.11a/b/g)[1]. The desired multi-band operation can be achieved by using switchable L-C resonators in one VCO core, and the switched-capacitor bank with the adaptive frequency calibration (AFC) technique can reduce the VCO gain for low phase noise.

The essential function of the AFC is to determine the oscillation frequency is faster or slower than the desired VCO frequency, and generate the code for the target bank. The AFC time to select a proper VCO transfer curve should be minimized for fast settling time[2, 3].

In this paper, we present a CMOS LC VCO for universal wireless LAN applications which is designed in 1.8V 0.18μm CMOS process. The possible operation is verified for 5.8GHz band (5.725~

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5.825GHz), 5.2GHz band (5.150~5.325GHz), and 2.4GHz band (2.412~2.484GHz) using the switchable L-C resonators. To linearize its frequency-voltage gain, optimized multiple MOS varactor biasing technique is used for capacitance linearization. In order to operate in a wide-band frequency range with reduced VCO gain, 4-bit digitally controlled switched-capacitor bank is used and a wide-range digital logic quadricorrelator (WDLQ) is adopted for frequency detector to implement the AFC technique and binary search algorithm is used for the code decision state machine.

II. Design of Tri-Mode VCO

Fig. 1 shows the circuit schematic and layout of the designed CMOS LC VCO for IEEE 802.11a/b/g wireless LAN standards. PMOS transistors are chosen for VCO core and 4-bit switched-capacitor bank is used for reduced VCO phase noise as shown in fig. 2. The switchable L-C resonators are used to cover the tri-mode frequency bands. Band selection with L-C switching is shown in Table 1.

To linearize its frequency-voltage gain (Kvco), the capacitance linearization circuit using three varactor bias voltages is used as shown in fig. 3. With the bias voltage of 0V, the capacitance has a linear range in low voltage. It has a linear range in middle voltage with 0.9V bias voltage, and a linear range in high voltage with 1.8V bias voltage. Therefore, if three curves of different bias voltages (0V, 0.9V and 1.8V) are superposed, we can get the linearized C-V curve for the whole range. Fig. 4 shows the linearized C-V curve of the proposed design.

표 1. L-C 스위칭에 의한 대역 선택
Table 1. Band selection with L-C switching.

Vsw0	Vsw1	Valid L and C	Freq. Band [GHz]
HIGH	LOW	L0, L1, Cv	5.725~5.825
HIGH	HIGH	L0, L1, Cv, C0, C1	5.150~5.325
LOW	LOW	L0, L1, L2, L3, Cv	2.412~2.484

The unit capacitance should be carefully decided to cover the required frequency band, and the NMOS switch array as well as the capacitor array are binary-weighted for proper operation.

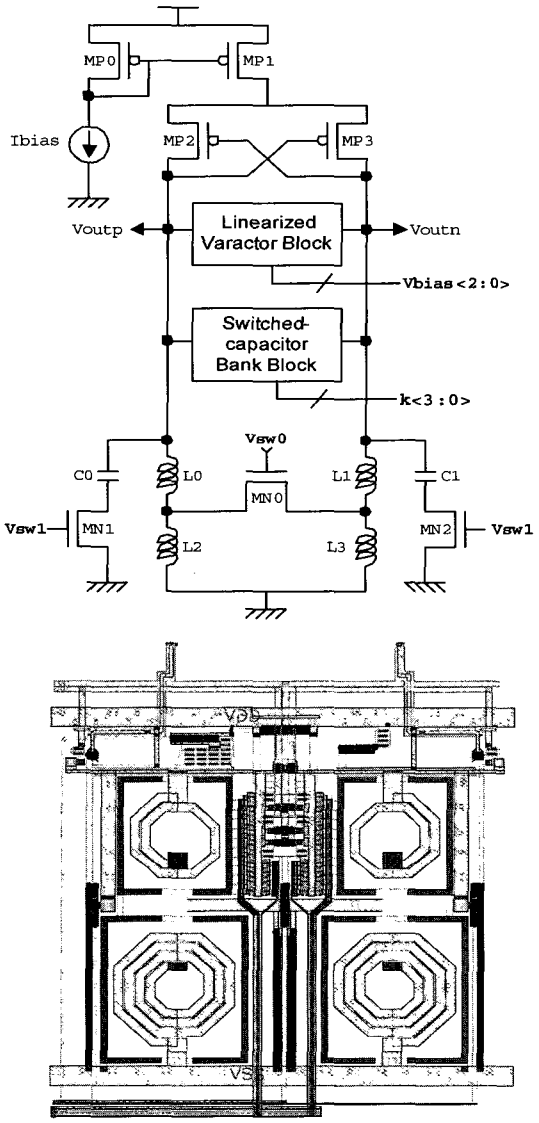


그림 1. L-C 스위칭 기법으로 설계된 VCO 회로도 및 레이아웃
Fig. 1. Circuit schematic and layout of the designed VCO with the switchable L-C resonators.

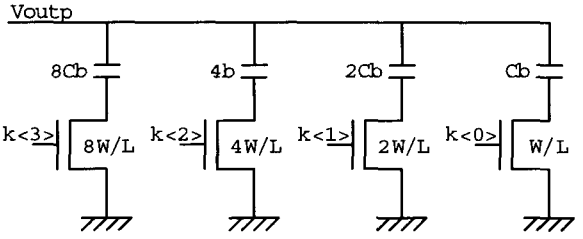


그림 2. 캐패시터 뱅크 구조
Fig. 2. Switched-capacitor bank configuration.

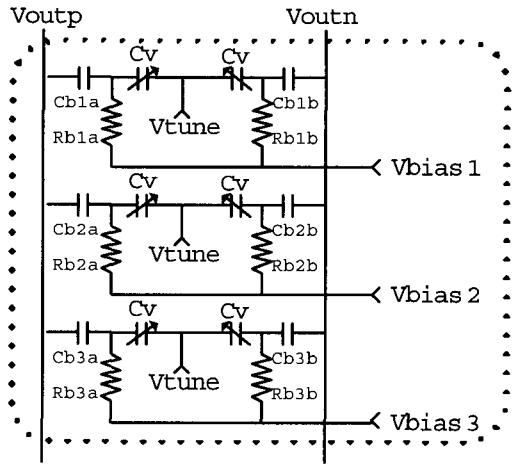


그림 3. 선형화된 버랙터 블록
Fig. 3. Linearized varactor block.

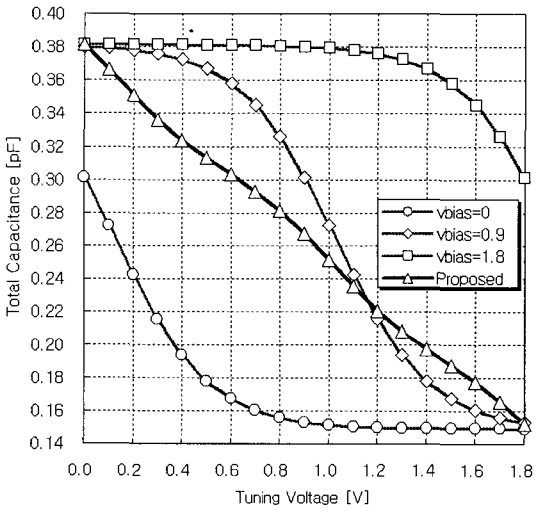


그림 4 선형화된 C-V 특성
Fig. 4. Linearized C-V curve.

III. Design of WDLQ-based AFC

The AFC block is used to select the proper transfer curve among the many curves of the switched-capacitor bank VCO. The AFC technique is used for not only extending the frequency band of the VCO but also reducing the lock time of the phase-locked loop based frequency synthesizer.

Early approach to the detection of frequency was based on the comparison of the frequency of the reference clock and the VCO feedback clock using counters and state machine to determine which clock is faster.

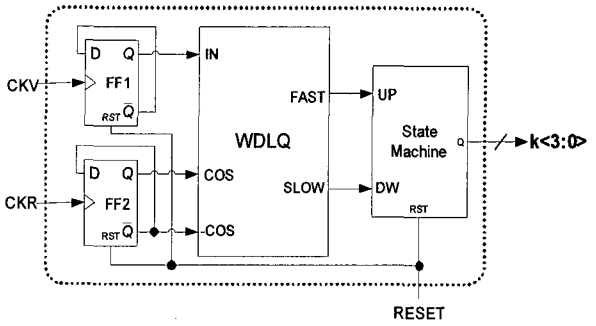


그림 5. WDLQ에 기반한 AFC 블록도
Fig. 5. Block diagram of WDLQ-based AFC.

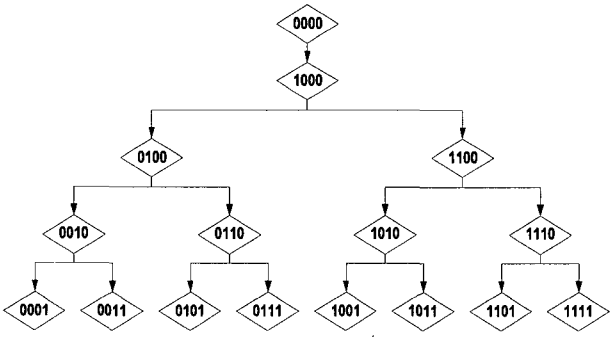


그림 6. 이진 검색 알고리듬에 의한 상태 변환
Fig. 6. State machine using binary search algorithm.

In this paper, we adopt a wide-range digital logic quadricorrelator (WDLQ) for frequency detector to implement the AFC and use a state machine for code decision logic as shown in fig. 5.

Front-end D-FFs (FF1,2) are used to make the VCO feedback clock (CKV) and the reference clock (CKR) signals have 50% duty cycle, which is desired for proper WDLQ operation. The state machine uses a pulse on the FAST port as an up count signal and a pulse on the SLOW port as a down count signal, and completes the code value k[3:0] to select the proper bank frequency using binary search algorithm as shown in fig. 6. The binary search algorithm can shorten the AFC time to determine the control bit of the AFC. When the frequency difference of these two input signals, CKR and CKV, is within a certain frequency resolution, this binary search can end and the AFC operation is completed.

The WDLQ has been extended from a digital logic quadricorrelator (DLQ) whose operation is based on Teager's analog energy tracker[4]. The WDLQ circuit has wide detection range of ±100% of the reference

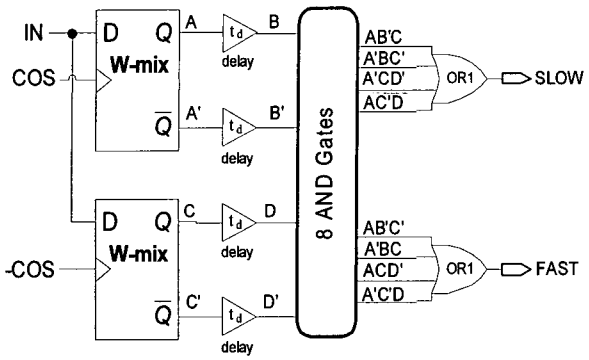


그림 7. 광역 직교상관기 (WDLQ)
Fig. 7. Wide-range DLQ (WDLQ).

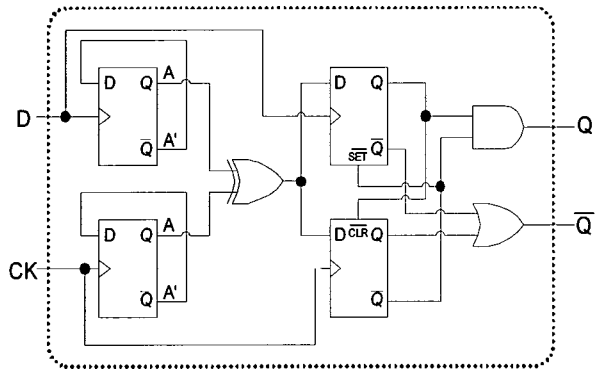


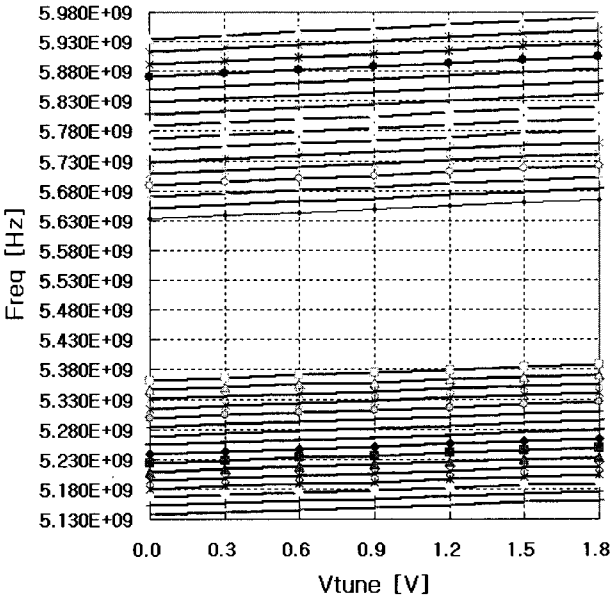
그림 8. 광역 믹서
Fig. 8. Wide-range mixer.

clock rate, and fast response time, so it is suitable for fast frequency detector, which is the main concern in the implementation of the fast AFC block. A configuration of a wide-range DLQ (WDLQ) is shown in Fig. 7. Front-end D-FFs are wide-range mixers as shown in Fig. 8.

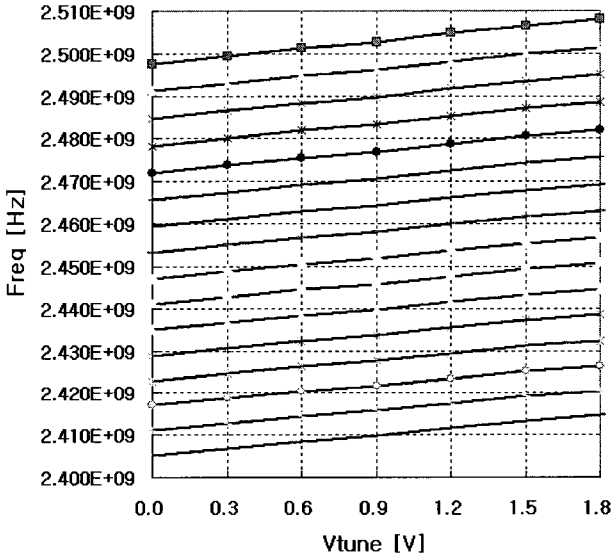
IV. Simulation Results

The proposed VCO was designed using ADS, and fig. 9(a)~(b) show the VCO transfer curve simulation results.

The sixteen curves of each frequency band show the possible operation for 5.8GHz band (5.725~5.825GHz), 5.2GHz band (5.150~5.325GHz), and 2.4GHz band (2.412~2.484GHz) with a tuning voltage from 0 to 1.8V. As shown in the figures, the curves of each band are partially overlapping for the design margin, and the linearized characteristics can also help the stable operation of the AFC block.



(a) 5.8GHz band and 5.2GHz band



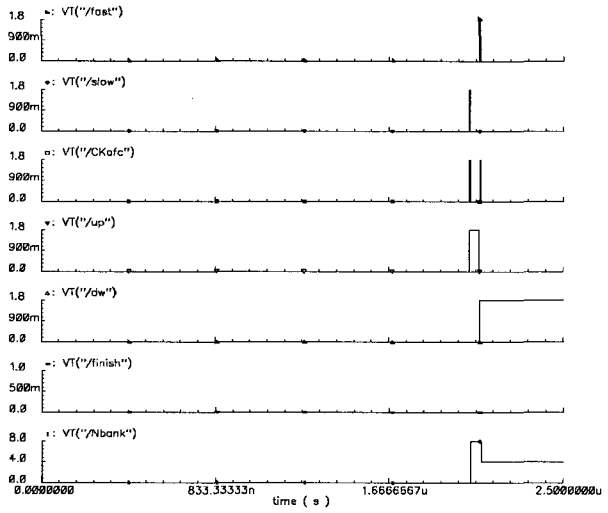
(b) 2.4GHz band

그림 9. VCO의 주파수 특성
Fig. 9. Frequency characteristics of the VCO.

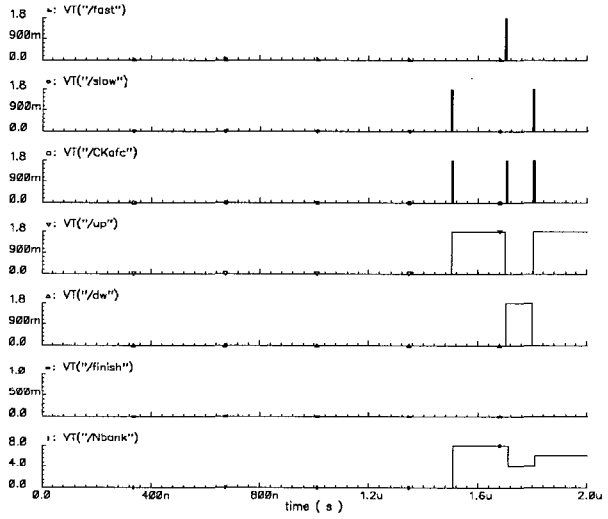
The CADENCE Spectre simulation results of the proposed AFC block for each band are shown in fig. 10(a)~(c). The AFC code value can be estimated by

$$N_{bank} = k<3:0> = \frac{F_{ref} \times N - F_o - K_{VCO} \times 0.9}{F_{step}}$$

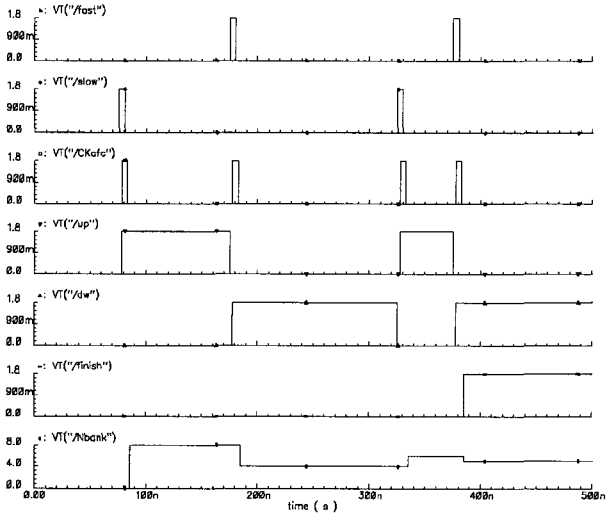
The code decision operation is finalized in less than 2.5μs with 40 MHz reference clock, which is shortened by almost a third in comparison with the previous works.



(a) N=143, Ftarget=5.72GHz, Nbank=4 (0→8→4)



(b) N=131, Ftarget=5.24GHz, Nbank=6 (0→8→4→6)



(c) N=61, Ftarget=2.44GHz, Nbank=5 (0→8→4→6→5)

그림 10. AFC 블록의 코드 결정 동작
Fig. 10. Code decision operation of the AFC block.

V. Conclusion

CMOS LC VCO with fast AFC technique for IEEE 802.11a/b/g wireless LAN applications was designed in 1.8V 0.18μm CMOS process. The possible operation was verified for 5.8GHz, 5.2GHz, and 2.4GHz band using the switchable L-C resonators. 4-bit switched-capacitor bank was used for each band and a WDLQ-based binary search state machine was adopted to implement the fast response AFC technique.

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