A Dual-band Fractional-N Frequency Synthesizer for 2GHz and 5GHz

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Abstract: A new dual-band fractional-N frequency synthesizer is designed to support both 2GHz and 5GHz.

The frequencies of two bands are synthesized by single PLL. It needs only a few additional circuits for dual band and has advantages in power and chip area. The synthesizer is composed of dual-band VCO, prescaler, 8/9 divider, PFD(phase-frequency detector), Charge Pump and LF(loop filter).

0.18*um* CMOS process with 1.8V supply voltage is used in design. SPICE and ADS simulation is performed using the layout extracted net-list.

The proposed synthesizer is applicable to IEEE. std 802.11a/b.

1. INSTRUCTION

WLAN(Wireless LAN) gives practical convenience to users and is applicable to various products, and the commercial value of WLAN is increasing nowaday.

WLAN standards include IEEE std. 802.11a/b and etc., which are composed of 5GHz-band and 2GHz-band. Accordingly, to meet each WLAN standard, we need separate frequency synthesizer for different bands. This work proposes a new architecture for fractional-N frequency synthesizer to support two bands in single frequency synthesizer using 2GHz/5GHz dual-band VCO and low value divider.

The proposed architecture has many advantages owing to using only one PLL loop. SPICE and ADS simulation is carried out after the layout parasitic extraction to verify the operation of frequency synthesizer.

2. THE PROPOSED ARCHITECTURE OF FRACTIONAL-N FREQUENCY SYNTHESIZER

The popular frequency synthesizer are an integer type and a fractional type, and we adopted fractional-N type in this work. The Fractional-N frequency synthesizer could adjust the dividing rate of N/N+1 divider precisely using sigma-delta modulator, accumulator or counter. Therefore when the channel space is narrow, it is easily possible to synthesize frequency using fractional type, comparing to integer type with the relatively high dividing value. The fractional-N type has a lower dividing value, so the phase noise in given bands is depressed. This architecture also decreases a spurious tone in PLL-loop because of using a higher value for reference frequency.[1][2]

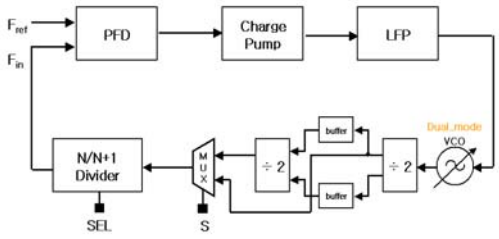

Fig. 1 Structure of proposed frequency synthesizer

Fig. 1 shows the proposed architecture of dual-band frequency synthesizer. The VCO(voltage controlled oscillator) operates 2GHz-band and 5GHz-band which is designed through collaboration. In the prescaler which is directly connected to VCO, the frequency is divided by 2 or 4, afterward the divided outputs are

selected by MUX. These blocks construct dual-band mode in one-PLL loop. In other words, when the output of VCO output goes through prescaler block, 5GHz-band signal goes by way of two 2 divider and 2GHz-band signal by way of one 2 divider and thereafter one of two divided output delivers 8/9 divider(N/N+1 divider) input signal by MUX selectively.

Table 1. shows channel frequency, output frequency of prescaler and needed dividing value for generating desired channel frequency. The proposed architecture could support dual-band frequency synthesis, because the dividing value lies in between 8 and 9 as shown in Table 1.

Table. 1 IEEE std. 802.11a/b specification and calculated value for supporting the proposed architecture.

design spec [MHz}	presca-ler (/2)	dividing value	design spec [MHz]	prescaler		dividing value
				/2	/2	
2412	1206	8.04000	5180	2590	1295	8.63333
2417	1208.5	8.05667	5200	2600	1300	8.66667
2422	1211	8.07333	5220	2610	1305	8.7
2427	1213.5	8.09000	5240	2620	1310	8.73333
2432	1216	8.10667	5260	2630	1315	8.76667
2437	1218.5	8.12333	5280	2640	1320	8.8
2442	1221	8.14000	5300	2650	1325	8.83333
2447	1223.5	8.15667	5320	2660	1330	8.86667
2452	1226	8.17333				
2457	1228.5	8.19000				
2462	1231	8.20667				
2467	1233.5	8.22333				
2472	1236	8.24000				
2484	1242	8.28000				

5180MHz, the first channel in the 5GHz-band which is generated by VCO, is divided by 4 in the prescaler. The output of prescaler is 1295MHz and this signal is divided through 8/9 divider.

The reference frequency which is used as the input of PFD is 150MHz and 8/9 divider should accomplish about 8.63333 dividing value which is synthesized by 63% operation of divider 9 and 37% operation of divider 8. This divided signal is used as the input of PFD(F_{in}), and then the other input, F_{ref}(reference frequency) is 150MHz as mentioned above. F_{ref} calculated to support IEEE 802.11a/b standard considering the dividing range of 8/9 divider.[3]

The outputs of PFD show the phase-frequency difference between F_{ref} and the divided output of VCO. Charge pump receives the outputs of PFD and controls the charging and discharging current. The output of LF generates DC voltage which supplies the control signal of VCO. These operations make PLL loop to lock the frequency of VCO with the reference frequency.

The control of dividing value is accomplished by selecting dividing value of 8/9 divider using the sigma-delta modulator. The sigma-delta modulator is designed using the 3th-order single structure. The data width is 16bits and VHDL is used for modulator design. The verification of sigma-delta modulator was completed by Xilinx FPGA.[4]

3. BLOCK DESIGN OF FREQUENCY SYNTHESIZER

Fig. 2 is the structure of 8/9 divider for frequency synthesis. Fig. 3 shows the PFD circuit and the PFD generates output signals about the phase-frequency difference between both inputs. Fig. 4 shows D Flip-Flop used in 8/9 divider which is selected to operate at high frequency range.

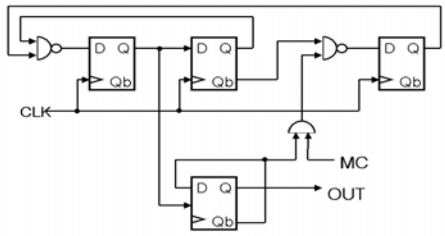

Fig. 2 8/9 divider

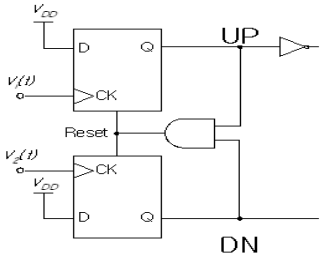

Fig. 3 PFD

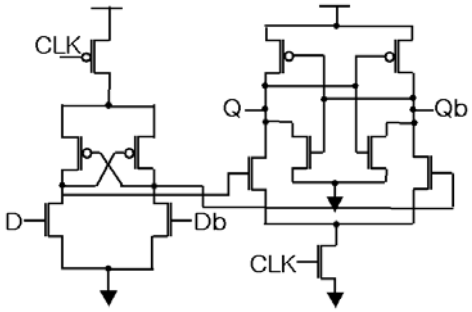

Fig. 4 High speed D-F/F used in 8/9 divider

The charge pump circuit in Fig. 5 charges or discharges the current of output node according to the UP/DOWN signals. The charge pump is designed to balance charging and discharging current and the pumping current is about 50*uA*. The loop filter consists of two resistors and three capacitors and is designed as the 3rd-order passive filter.

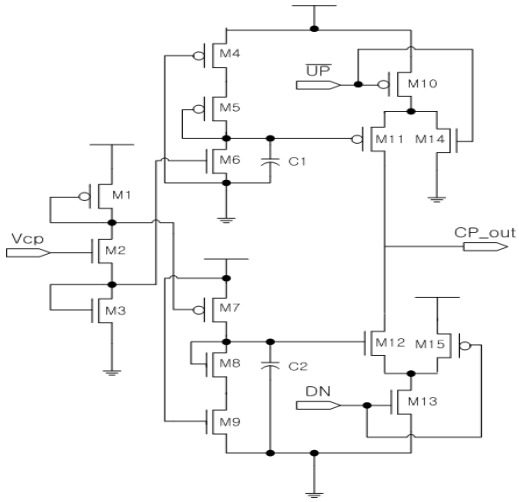

Fig. 5 Charge pump

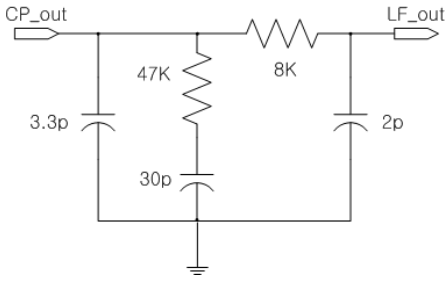

Fig. 6 Loop filter

4. SIMULATION AND LAYOUT

The frequency synthesizer supporting both 2GHz -band and 5GHz-band is designed using 0.18*um* CMOS process and 1.8V supply voltage is used.

After the frequency synthesizer was designed, the net-list including the layout parasitic is verified using HSPICE simulation. ADS simulation is carried out for VCO and prescaler, because its operating range lies in RF band.

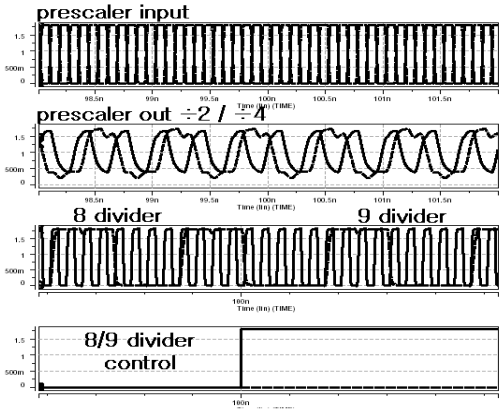

Fig. 7 Prescaler and 8/9 divider simulation by SPICE

Fig. 7 is the SPICE simulation result of prescaler and divider. The prescaler operates as 2 or 4 divider and 8/9 divider operates as 8 divider or 9 divider according to the control signal.

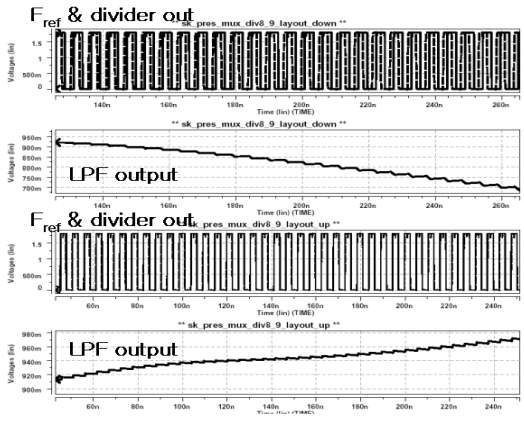

Fig. 8 VCO control signal (LF output)

Fig. 8 shows the simulation result of PFD, charge pump and LF. The difference between two inputs of PFD is detected and the output of PFD connected to charge-pump and LF. The final output of the above block is the VCO control voltage which increases or decrease slowly according to the two input signals of

PFD.

Fig. 9 shows the layout of PLL core for frequency synthesizer and Fig. 10 is the full chip layout of frequency synthesizer.

The chip area excluding PADs is about 1.2mm x 1.2mm. The full-chip includes the frequency synthesizer and PLL core for test.

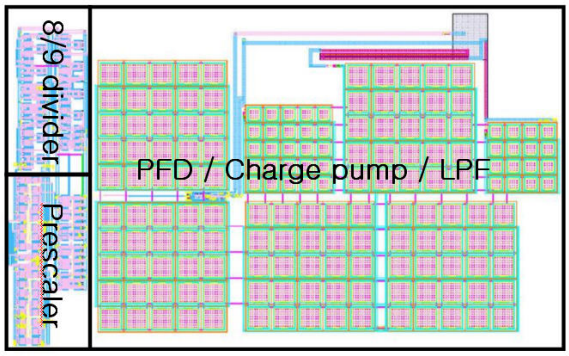

Fig. 9 The layout of PLL core for frequency synthesizer

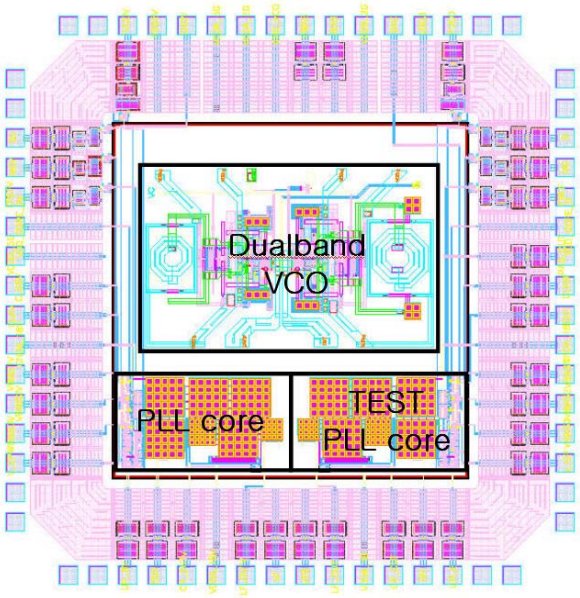

Fig. 10 Full-chip Layout

5. CONCLUSION

This paper proposed the improved architecture of fractional-N frequency synthesizer to support 2GHz-band and 5GHz-band at the same time and is applicable to IEEE std. 802.11a/b. The proposed frequency synthesizer has advantages of depressing phase noise and spurious tone problem. The proposed architecture uses only one-VCO and one-PLL loop for two standards of WLAN, so complex additional block is not needed for dual-band support. In others words, another spacious VCO and additional block is not needed, so it has advantages in power consumption and chip area.

The designed frequency synthesizer for dual-band is under fabrication using 0.18*um* 1-poly 6-metal CMOS process. The supply voltage of I/O block is 3.3V and the core supply is 1.8V. The TQFP(Thin Quad Flat Pack) package is selected and the number of pins is 64. CAD tools in this work are supported by IDEC (IC Design Education Center).

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