A Study on 11 MHz ~ 1537 MHz DCO using Tri-state Inverter for DAB application

Byeung-geon Jeon[1] and Yong Moon[2]
Department of Electronic Engineering
Soongsil University
Seoul, South Korea
eoenqudrjs@hanmail.net[1]
moony@ssu.ac.kr[2]

Tae-won Ahn
Department of Electronic Engineering
Dongyang Technical College
Seoul, South Korea
twahn@dongyang.ac.kr

***Abstract*—Digitally Controlled Oscillator (DCO) for Digital Audio Broadcasting (DAB) is proposed using 0.18 µm CMOS process parameters with 1.8 V supply voltage. In this paper, the proposed DCO consist of tri-state inverter array and calibration block. Tri-state inverter array is 5-stage ring oscillator and each stage has 160 tri-state inverters. Calibration block is composed of 64 NMOS pass transistors and 64 Metal-Insulator-Metal (MIM) capacitors with different values. The proposed DCO has the frequency tuning range from 10.5088 MHz to 1537.32 MHz by controlling 800 tri-state inverters. BAND-III (174.928 MHz ~ 239.200 MHz) and L-BAND (1452.960 MHz ~ 1492.624 MHz) are synthesized for DAB application. In order to synthesize channel frequency for DAB system, tri-state inverter array that adjusts frequency coarsely and calibration block that adjusts frequency finely have to work together and both of them are controlled by 6-bit digital word. So the proposed DCO could tune frequencies of 64 channels for DAB accurately. It has simulated phase noise of -114.93 dBc/Hz at 1MHz offset and power consumption of 3.28 mW at 174.928 MHz. And it has simulated phase noise of -106.35 dBc/Hz at 1MHz offset and power consumption of 25.77 mW at 1490.624 MHz.**

Keywords-Digitally Controlled Oscillator (DCO), Ring Oscillator, Tri-state Inverter, Metal-Insulator-Metal (MIM) Capacitor, Digital Audio Broadcasting (DAB)

I. INTRODUCTION

The Digital Audio Broadcasting (DAB) that has been started in England since mid 19th's is a broadcasting service provided by many countries including Europe, America, Japan, South Korea and so on. As an audio broadcasting adopts digitization, DAB offers CD quality sound, excellent mobile communication quality, interactive-directional communication, various data service and so on, though DAB uses such as AM/FM, short-wave/ medium-wave/ long-wave broadcasting [1][2]. The frequency bandwidth that is defined in the DAB standard is 1.536 MHz and MPEG Audio Layer II is used for audio coding. The frequency bands for DAB system are BAND-III (174.928 MHz ~ 239.200 MHz) and L-BAND (1452.960 MHz ~ 1490. 624 MHz) [3][4]. The characteristics of BAND-III include excellent propagation quality and short length antenna which is useful in system implementation. So it is regarded as the optimal terrestrial DAB frequency range. Also, L-BAND could accommodate numerous broadcasting programs due to large bandwidth and is used as mixed satellite /terrestrial or local broadcasting applications [5].

The frequencies of BAND-III and L-BAND having these properties could be generated by ring type oscillator. The period of oscillation is varied either by changing the number of inverter stages in the ring oscillator or varying the propagation delay of inverter. It is clear that the frequency of oscillation without changing number of stages can be varied either by changing the load capacitance or current driving strength to the load. The propagation delay of inverter is proportional to (W/L) ratio of the transistor as widening width increases the capacitance and decreases the resistance. The load capacitance can be changed by using Metal-Insulator-Metal (MIM) capacitor or MOS transistor [6][7] at the output node of ring oscillator. This approach might not be useful in sub-micron technology as wired capacitance have significant portion in load capacitance, which in turn, limit the maximum oscillating frequency [8] of an oscillator. In other word, it would not be useful to achieve wide tuning range of an oscillator. But it could be much useful approach to synthesize channel frequencies assigned to DAB, because the major part of interest and the objective of the presented DCO are not wide tuning range but accurate synthesis of the frequency for DAB. Controlling delay by changing the driving current would support various frequencies and controlling delay by changing the load capacitance with MIM capacitor that allows for fine frequency control would provide an approach to the accurate frequency adjustment in the presented DCO.

In this paper, we have designed and verified the DCO that could generate the frequencies of 41 channels assigned to BAND-III band and the frequencies of 23 channels assigned to L-BAND band in DAB.

The paper is organized as follows. Section II describes and explains about the architecture and schematic-level design of the proposed DCO. Simulation results are shown in Section III. Section IV presents a summary and conclusions regarding this work, finally.

II. A DESIGN OF DCO FOR DAB SYSTEM

The DCO that adapts conventional ring oscillator type was designed to have wide tuning range and synthesize frequencies linearly according to control code. By the way, conventional

DCO could not synthesize the frequencies of 64-channels assigned to DAB accurately by the linear property of ring oscillator type DCO. In particular, frequency step between channels of BAND-III has inconstant frequency step values such as 0.16 MHz, 1.552 MHz, 1.568 MHz, 1.712 MHz and 1.872 MHz. Because of this reason, exact channel frequencies assigned to BAND-III could not be generated even if DCO has high accurate frequency steps with long control word. The proposed DCO for DAB system is designed to generate frequencies of 41 channels assigned to BAND-III that has problem above and frequencies of 23 channels assigned to L-BAND that has the frequency step of 1.712 MHz between adjacent channels

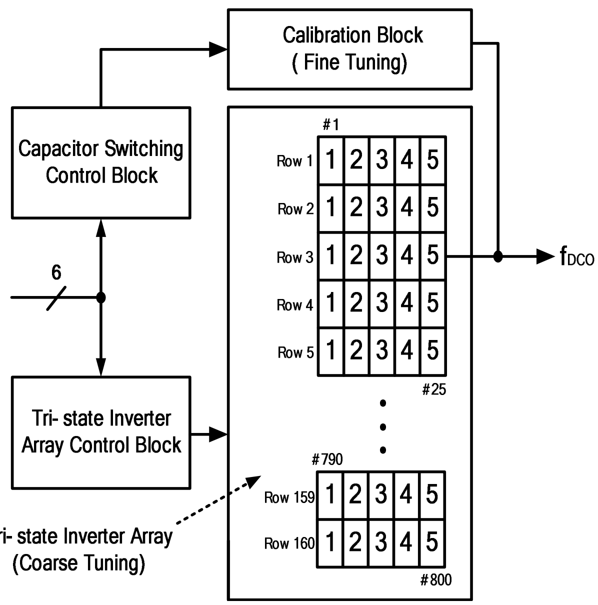

Figure 1. Block diagram of the DCO

Fig. 1 shows the block diagram of proposed DCO for DAB system. In macro view, the DCO consist of the tri-state inverter array block that adjusts frequency coarsely at first and the calibration block that controls frequency finely by switching MIM capacitor selectively. In the tri-state inverter array of the DCO based on ring oscillator which is used in this work, the inverters that comprise the ring are divided into addressable component structures to be controlled digitally and the effective strength of the composite inverters is adjusted by increasing or decreasing the number of enabled transistors that form each stage of ring oscillator [9]. The effective strength of the calibration block is adjusted digitally by turning on one pass transistor at a time. The control block is used to operate the tri-state inverter array and calibration block digitally. The decoder having thermometer control structure is used as the tri-state inverter array control block and the decoder having general structure is used as the capacitor switching control block.

In this work, we could digitally control every frequency of channel assigned to DAB system by just 6-bit, because the proposed DCO has only to synthesize frequencies of 64-channels assigned to BAND-III and L-BAND for DAB system.

Fig. 2 shows the structure of tri-state inverter array that adjusts the frequency coarsely at first. Each stage of this five-stage ring oscillator is comprised of 160 tri-state CMOS inverters connected in parallel, so total number of inverters are 800. Five tri-state inverters in row 1 of tri-state inverter array are always tuned on to provide reliable startup and operation, when none of tri-state inverters in the remaining rows are turned on [9]. The sizes of tri-state inverter are uniform, and chosen to generate desired frequencies.

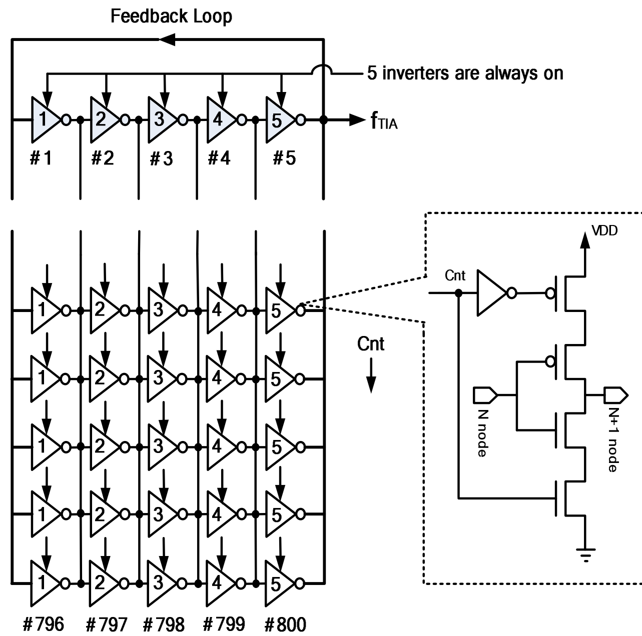

Figure 2. The schematic of tri-state inverter array

The operation of tri-state inverter array is as follows. As more tri-state inverters in tri-state inverter array are turned on by tri-state inverter array control block, the current driving strength in the loop of tri-state inverter array increases while load capacitance in tri-state inverter array remains constant, resulting in the increase of f_{TIA} (output frequency of tri-state inverter array) by decreasing delay time that charge or discharge an inverter load capacitance in tri-state inverter array [9][10]. On the contrary, as more tri-state inverters in loop of tri-state inverter array are turned off, the current driving strength of the loop of tri-state inverter array decreases while load capacitance in inverter array remains constant and f_{TIA} decrease by increasing the delay time that charge or discharge inverter load capacitance in tri-state inverter array.

When 6 tri-state inverters are turned on in tri-state inverter array, f_{TIA} has the value of 10.2088 MHz. When all tri-state inverters (800) turned on, f_{TIA} is 1537.32 MHz. Because each stage of ring oscillator has 159 controllable inverters which is connected in parallel, tri-state inverter array creates 795 discrete frequencies. When the number of turned on tri-state inverters out of 800 inverters in tri-state inverter array lies in between 89 and 121, the approximate frequency of BAND-III is generated. The frequency of f_{TIA} increases as the number of turned on inverters are increasing. Whenever one inverter is turned on at a time, the frequency steps of the inverter array have different values about 1.949 MHz ~ 2.2254 MHz. Also, when the number of turned on tri-state inverters lies in between 753 and 775, the approximate frequency of L-BAND is generated. Whenever one inverter is turned one at a time, the frequency steps of the inverter array have different values about 1.664 MHz ~ 1.686 MHz. As described above, f_{TIA} have various frequency values by controlling the number of inverter turned on. But the frequency step is not constant, so the frequencies allocated to DAB which require high degree of accuracy could not be set precisely in a detailed unit such as 1 KHz. First of all, to solve this problem, we can adjust f_{TIA} close to the target frequency dedicated to the channel of DAB and then calibrate it with NMOS switches and MIM capacitors of 64, respectively, by connecting a capacitor selectively. This approach is shown in Fig. 3.

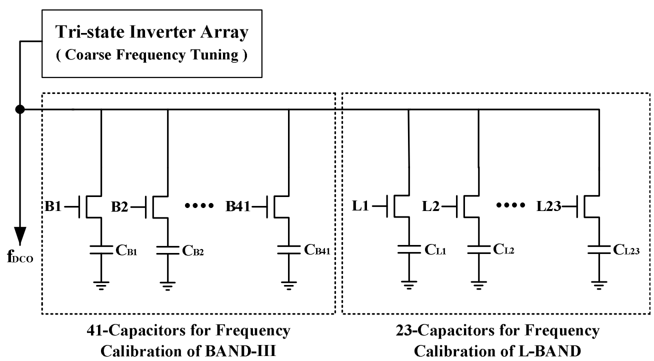

Figure 3. Frequency calibration block for fine tuning

In this case, the width of NMOS switches are 2.63 μm and the capacitance of MIM capacitors have different values. The number of tri-state inverters that are turned on is fixed, so the current driving strength of DCO does not change. Total load capacitance of DCO, however, increases by turning on pass transistors which connect MIM capacitors and output node of tri-state inverter array selectively. In result, the delay time increases due to the increased total load capacitance of DCO, and the output frequency of DCO (f_{DCO}) is decreased. As the more capacitance of MIM capacitor connected with NMOS switch is chosen strictly, the DCO could synthesize the output frequency corresponding to DAB channels accurately. The frequency difference (Δf) corresponding to the constant capacitance of capacitor is varied according to the number of tri-state inverters turned on. For example, when 753 tri-state inverters are turned on in inverter array, Δf is 3.97 MHz for the capacitance of 25 fF. When 121 tri-state inverters are turned on in inverter array, Δf is 0.93 MHz for the same capacitance. In brief, the frequency variation increases as the number of tri-state inverter which is turned on increases with the same capacitance value.

III. SIMULATION RESULT

The DCO is designed using 0.18 μm CMOS process and verified by SPECTRE. Fig. 4 and Fig. 5 show the synthesized frequencies according to digital control word. The simulation results are shown in this section.

Fig. 4 shows the generated frequency of BAND-III according to digital control word. Frequency steps between channels of BAND-III have inconstant value. Channel frequencies assigned to BAND-III is synthesized exactly by using MIM capacitors having the capacitance between 7 fF and 90 fF.

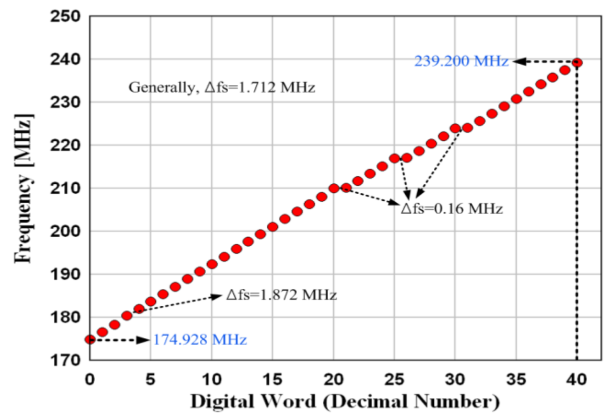

Figure 4. BAND-III frequency versus digital word

Fig. 5 shows the generated frequency of L-BAND according to digital control word. The Frequency step between channels of L-BAND is constant. The frequency step of channel frequencies assigned to L-BAND is 1.712 MHz. Because frequency step is constant, capacitors that have not significant differences could generate the frequencies assigned to L-BAND. The capacitance of used MIM capacitor for L-BAND has the value between 22.4 fF and 26.28 fF.

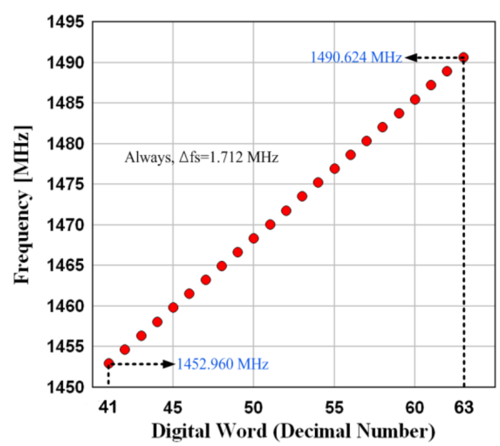

Figure 5. L-BAND frequency versus digital word

Fig. 6 shows the way how the frequency of 13E channel assigned to BAND-III can be tuned. At first, f_{TIA} is 238.469 MHz when 120 tri-state inverters in tri-state inverter array are turned on. This frequency is 0.981 MHz higher than the frequency of 13E channel (237.488 MHz). To decrease the frequency as this amount (Δf = 0.981 MHz), calibration block do the role by switching the MIM capacitor which has the capacitance of 27.8 fF. Then, the proposed DCO synthesizes the exact frequency of 13E channel (237.488 MHz).

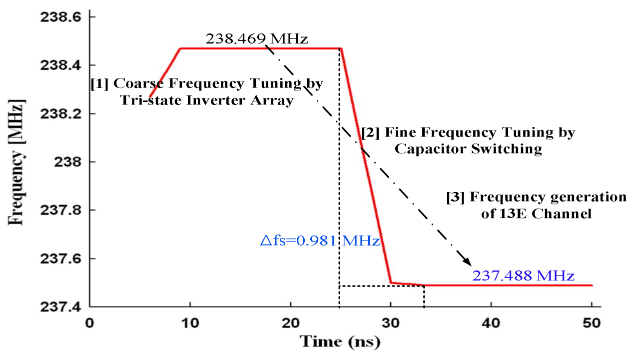

Figure 6. Frequency generation procedure of 13E channel

The conditions to synthesize channel frequencies of DAB are summarized in Table I.

TABLE I
THE CONDITIONS TO SYNTHESIZE CHANNEL FREQUENCIES OF DAB

BAND of DAB	BAND−Ⅲ		L-BAND	
Sub-BAND NAME	5A	13F	LA	LW
Channel Frequency	174.928 MHz	239.2 MHz	1452.96 MHz	1490.624 MHz
The Number of Inverter Turned on out of 800	89	121	753	775
Value of Connected Capacitor	14.4 fF	36.82 fF	22.4 fF	26.28 fF
Synthesized Frequency [MHz]	174.92802 [MHz]	239.20011 [MHz]	1452.96047 [MHz]	1490.62398 [MHz]

Fig. 7 shows the frequency of 5A channel (174.928 MHz) generated in the proposed DCO. This frequency value is synthesized by turning on 89 tri-state inverters out of 800 inverters in tri-state inverter array and switching the capacitor having the capacitance of 14.4 fF in calibration block at the same time.

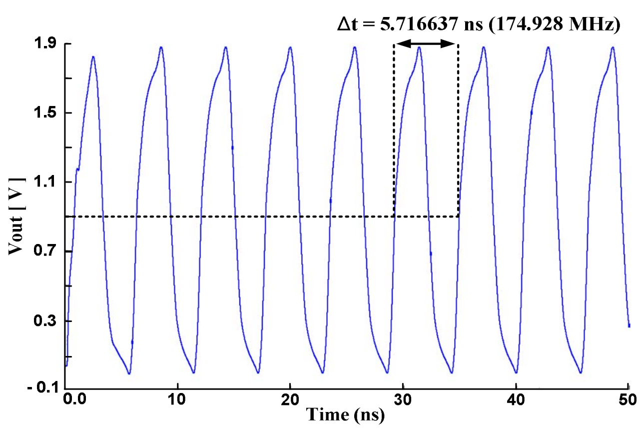

Figure 7. Simulation result of 5A channel frequency synthesis

Fig. 8 ~ Fig. 10 show the frequency of 13F channel, LA channel and LW channel generated in the proposed DCO, respectively.

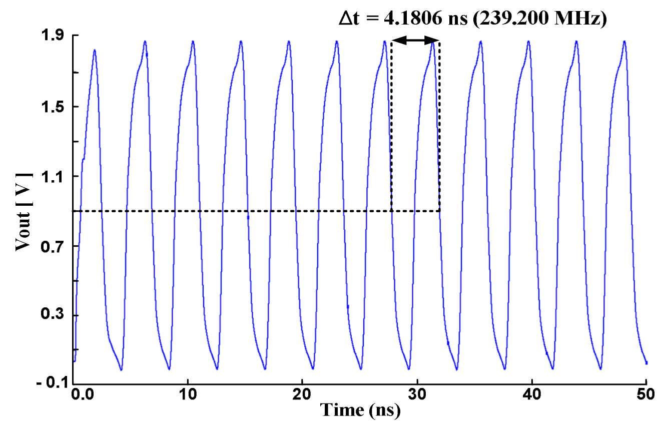

Figure 8. Simulation result of 13F channel frequency synthesis

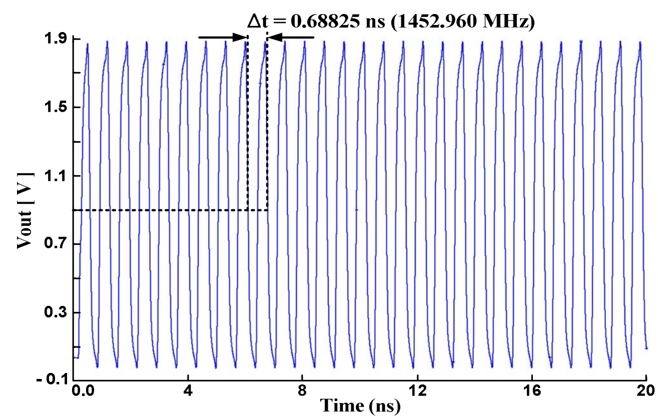

Figure 9. Simulation result of LA channel frequency synthesis

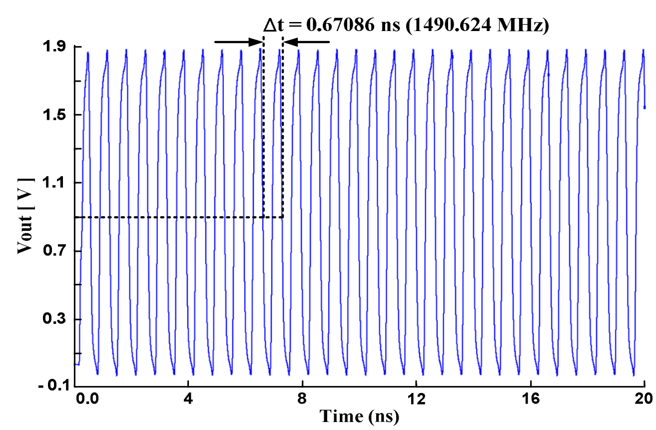

Figure 10. Simulation result of LW channel frequency synthesis

The current, power and phase noise according to channel frequency of DAB system are illustrated in Table II.

Fig. 11 and Fig. 12 show the simulated phase noise of the proposed DCO according to selected channel in each band. The simulated phase noise is -114.93 dBc/Hz for 5A channel (174.928 MHz) and -106.35 dBc/Hz for LW channel (1490. 624 MHz) at 1 MHz offset.

TABLE 2
THE CURRENT, POWER AND PHASE NOISE ACCORDING TO CHANNEL FREQUENCY OF DAB.

BAND of DAB	**BAND−Ⅲ**		**L−BAND**	
Sub-BAND NAME	**5A**	**13F**	**LA**	**LW**
Channel Frequency	174.928 MHz	239.2 MHz	1452.96 MHz	1490.624 MHz
Consumed Current	1.82 mA	2.56 mA	14.01 mA	14.4 mA
Power Consumption (1.8V Supply Voltage)	3.28 mW	4.58 mW	25.02 mW	25.77 mW
Phase Noise (1MHz offset)	-114.93 dBc/Hz	-113.6 dBc/Hz	-106.5 dBc/Hz	-106.35 dBc/Hz

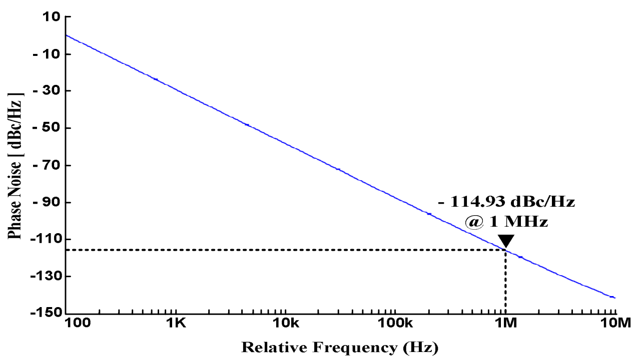

Figure 11. Simulated phase noise for 5A channel frequency

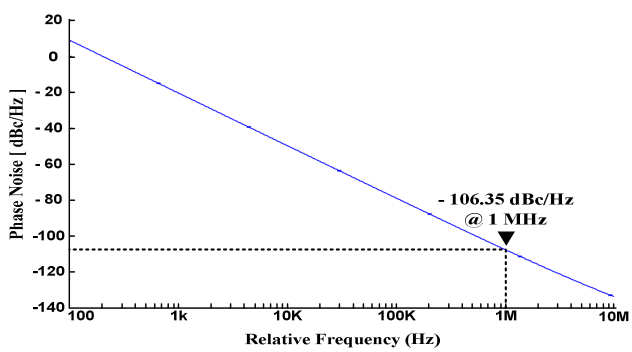

Figure 12. Simulated phase noise for LW channel frequency

IV. CONCLUSION

The 6-bit DCO for DAB-T (Eureka-147) and DAB-S application is designed using 0.18 μm CMOS process with 1.8 V supply voltage. The proposed DCO consists of 800 tri-state inverters, 64-NMOS switches and 64-MIM capacitors. By turning on tri-state inverters in inverter array and switching capacitors of calibration block selectively, the output frequency of DCO could synthesize the frequency of channel assigned to DAB system. The frequency of 41 channels in BAND-III could be generated by turning on tri-state inverters between 89 and 121 out of 800 and switching 41 capacitors selectively. The value of used capacitors is about 7 fF ~ 90 fF. Also, the frequency of 23 channels in L-BAND could be tuned by turning on tri-state inverters between 753 and 775 out of 800 and switching 23 capacitors selectively. The used capacitors have the values between 22.4 fF and 26.28 fF. The simulated phase noise is -114.93 dBc/Hz for 5A channel (174.928 MHz) and -106.35 dBc/Hz for LW channel (1490. 624 MHz) at 1 MHz offset. The consumed current is 1.82 mA for 5A channel and 14.4 mA for LW channel at 1.8V supply power.

In this work, the proposed DCO could synthesize the frequency of every channel assigned to DAB and shows the feasibility of the DCO based-on ring oscillator topology.

ACKNOWLEDGMENT

This work was sponsored by SoC Industry Promotion Center, Human Resource Development Project for IT-SoC Architect. CAD tools were supported by IDEC.

REFERENCES

[1] Hsiao Wei Su, Yi Ke Cui, Bao Yong, and Zhi Hua Wang, “A RF Front-End for Digital Audio Broadcasting (DAB),” ECCTD, pp. 176-179, Aug. 2007.

[2] Yen-Horng Chen, Shin-Fu Chen, Ching-Feng Lee, Kai-Cheung Juang, Yeong-Lin Yu, and Tzu-Yi Yang “A Highly Integrated Dual Band Receiver IC for DAB,” IEEE MTT-S International, pp. 1191-1195, June. 2005.

[3] ETSI EN 300 401 Vi.4.1, “Digital Audio Broadcasting (DAB) to mobile, portable and fixed receivers,” ETSI, Jan. 2006.

[4] ETSI TR 101 496-3 V1.1.2, “Digital Audio Broadcasting (DAB); Guidelines and rules for implementation and operation,” ETSI, May. 2001.

[5] Bonkee Kim, Tae Wook Kim, Youngho Cho, Min-Su Jeong, Seyeob Kim, Heeyong Yoo, Seong-Mo Moon, Tae-Ju Lee, Jin-Kyu Lim, and Boeun Kim “A 100mW Dual Band CMOS Mobile-TV Tuner IC for T-DMB/DAB and ISDB-T,” 2006-ISSCC, vol. 49, pp. 614-615, Feb. 2006.

[6] A. Tomar, R. K. Pokharel, O. Nizhnik, H. Kanaya, and K. Yoshida, “Design of 1.1 GHz Highly Linear Digitally-Controlled Ring Oscillator with Wide Tuning Range,” RFIT2007-IEEE International Workshop on Radio-Frequency Integration Technology, pp. 82-85, Dec. 2007.

[7] R. K. Pokharel, A. Tomar, H. Kanaya, and K. Yoshida, “Design of Highly Linear, 1GHz 8-bit Digitally-Controlled Ring Oscillator with Wide Tuning Range in 0.18μm CMOS Process,” Microwave Conference 2008 China-Japan Joint, pp. 623-626, Sept. 2008.

[8] S. M. Rezaul Hasan, and Nazmul Ula, “A 16-bit CMOS digitally controlled oscillator using a novel control scheme,” 4th IEEE International Symposium on Circuits and Systems (2006-MWSCAS’06), vol.1, pp. 680-684, Aug. 2006.

[9] J.A. Tierno, A. V. Rylyakov, and D. Friedman, “A Wide Power-Supply Range, Wide Tuning Range, All Static CMOS All Digital PLL in 65 nm SOI,” accepted for publication in IEEE J. Solid-State Circuit, vol. 43, pp. 42-51, Jan. 2008.

[10] A. V. Rylyakov, J. A. Tierno, and G. J. English, “A Wide Power – Supply Range (0.5 V-to-1.3 V) Wide Tuning Range (500 MHz-to-8 GHz) All-Static CMOS ADPLL in 65nm SOI,” ISSCC Dig. Tech. Papers, pp. 172-173, Feb. 2007.