A Study of Frequency Synthesizer for AT-DMB Applications

Jun Cheng, Sung Hoon Bang, Nak Yoon Kim , Yong Moon
Department of Electronic Engineering, Soongsil University, Seoul, South Korea
chengjungood@ssu.ac.kr
moony@ssu.ac.kr

Abstract

This paper introduces the design of the frequency synthesizer for AT-DMB. 0.18um CMOS process with 1.8V supply voltage is used for the frequency synthesizer and the frequency range is from 110MHz to 522MHz for AT-DMB applications. This frequency synthesizer has good linearity by controlling tail current and load concurrently.

Keywords: CMOS, Differential Ring Oscillator(Ring VCO), T-DMB.

1.Introduction

Along with the development of the communication technology, there are a lot of electronic products has been developed and widely used. Among them, T-DMB(Terrestrial Digital Multimedia Broad Casting) which is one of the mobile broadcasting systems is extended nowadays and needs 160MHz~240MHz frequency range. Therefore, in order to meet the spread of mobile TV signal, a frequency synthesizer of wide frequency range which could satisfy frequency range for mobile DTV is needed. To satisfy this requirement, a wide band frequency synthesizer is studied in this paper. There are three parts in this paper. The first part introduced the circuit design of each block of frequency synthesizer. The second part shows the simulation result, and the last part is conclusion.

2. Frequency synthesizer design

2.1 Basic architecture

The basic structure of frequency synthesizer is shown in Fig.1. Among them, VCO is the core of frequency synthesizer. The most frequently used VCO's fabricated in CMOS process is LC oscillators and ring oscillators. Although LC oscillators have advantages in phase noise suppression, it also has many disadvantages, such as large area, the difficulty of designing inductor with a high Q value in present CMOS process, and a narrow tuning range etc. On the contrary, CMOS ring oscillators have been used widely since it has smaller area, wide tuning rang, good linearity, and require no external device while it could be easily designed and fabricated in CMOS process. Among COMS ring oscillators, the differential ring oscillators are generally adopted in applications for precise frequency control.

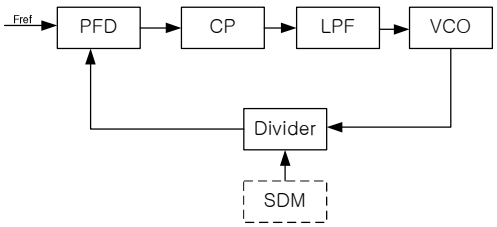
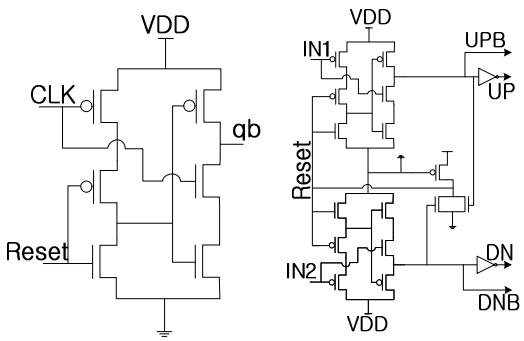


Fig.1. Block diagram of frequency synthesizer

2.2 The Design of PFD circuit

A conventional sequential type PFD(Phase Frequency Dector) structure is used in this study. The circuit is compose of two D flip-flop's circuits and a NOR gate. When the input signal has phase error with the reference signals, PFD generates UP or DOWN pulses which are the input signals of Charge pump. The reset signal will be generated when the input signal is equal to the reference signal. For improving the operation speed of circuit, we adopted the modified TSPC D flip-flop and a pseudo-NOR gate circuit.[1] The modified D flip-flop circuit and the proposed PFD circuit is shown in Fig.2.



(a) (b)

Fig.2. (a) Modified TSPC D flip-flop (b) PFD circuit

2.3 Charge pump and loop filter

The charge pump circuit is shown in Fig.3. From the schematic of charge pump, when up-switch is closed and

down-switch is open, the circuit perform charge operation, otherwise the circuit will discharge the charge of loop filter circuit. The charge pump circuit uses current mirror form and produce 60uA current flow, the current value can be adjusted by changing the value of resistance. We used the second order loop filter circuit in this paper.

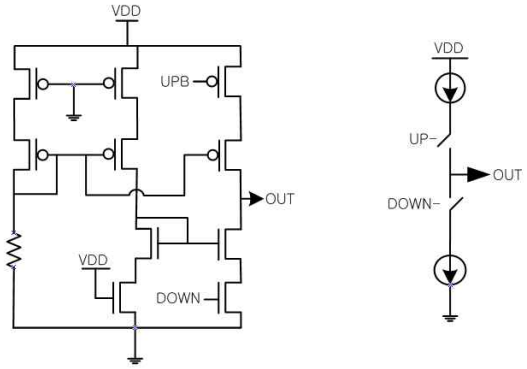


Fig.3. Charge pump basic circuit and the actual circuit

2.4 VCO

3 ways of load control are carried out to obtain a good linearity of VCO. The first of them is controlling load resistance by varying control voltage (A). And the second way is controlling the tail current flows by external voltage (B). The last one is controlling the load resistors and tail current at the same time by only one control voltage (C). The simulation result of 3 control method is shown in Fig.4.

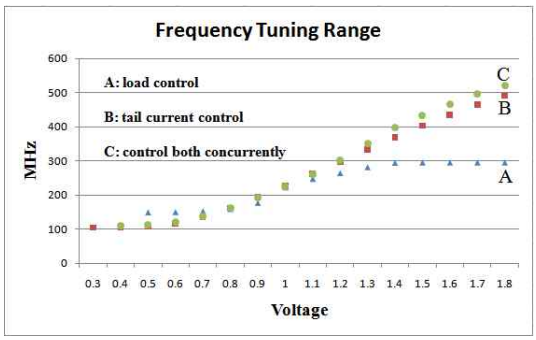


Fig.4. The simulation result of 3 control method

The result show that the curve A and C is better than curve B in linearity. And the curve C has wide frequency range. Analysis by simulation, the curve C is better than curve A and B in linearity and frequency range. So this paper selects a VCO with the bias circuit which controls the load resistor and tail current concurrently.

The block diagram of the proposed VCO including bias and buffer circuits is shown in Fig.5.

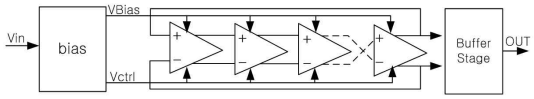


Fig.5. Block diagram of ring VCO

The ring oscillator is made of a number of delay stages, N which is decided by specification. Even number delay stage needs a wire inversion at the end. The output frequency of oscillator could use the following equation to calculate oscillation frequency.

$$f_{osc} \approx \frac{1}{2NC_L R_L} = \frac{I_{dd}}{2NC_L V_{SW}} \quad (1)$$

Where R_L, C_L is the total equivalent resistance and capacitance for the load, respectively. V_{sw} is the output amplitude of VCO，and I_{dd} is the charging current(tail current).

The ring VCO core consists of N delay cells which are modulated by the control voltage. For the needed frequency range, we used 7 stage ring oscillator form.[2]

2.4.1 Delay Cell circuit

The delay cell circuits generally have two types, one of them is called ‘triode load’, for which load elements are operated in the triode region, the other is called ‘symmetric load’ because the symmetry in its I-V characteristics has the good linearity of the loads. The triode delay cells consists of an NMOS source-coupled (MN1-MN2) differential pair which is operating in saturation region as shown in Fig.6(a).

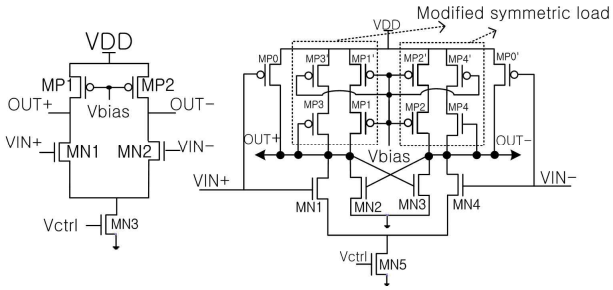


Fig.6. (a) Conventional delay cells with triode load, (b) The proposed delay cell

V_{ctrl} is the control voltage used to vary the frequency of oscillation . The delay of the delay cell is set by the charge in each node and the current through the triode load. In Fig.6(a), MP1 and MP2 are the load elements and are operated in the triode region. MN3 generates the tail current of the differential pair transistor MN1 and MN2 .

The triode load which uses MOSFETs biased in the

triode region exhibits poor linearity if frequency tuning range is large. Moreover, because the effective resistance of triode load is determined by the bias condition, $V_{dd} - V_{bias}$, the resistance is largely affected by the fluctuation of the supply voltage. Compared with triode loads, symmetric loads are less sensitive to the supply fluctuation, but its tuning range is very narrow. To achieve wide tuning-range, we used a new delay cell. The schematic of new delay cell is shown in Fig.6(b).

It includes two modified symmetric loads, positive partial feedback and two added PMOS MP0 and MP0'. The positive partial feedback which is generated by transistors MN2 and MN3 provides the required bias condition for the circuit to oscillate. Meanwhile, MP0 and MP0' are added to the delay cell of ring VCO to increase the operating frequency range.[2]

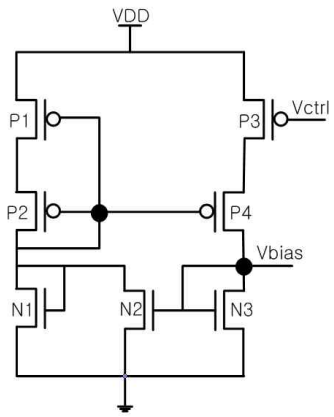


Fig.7. Bias circuit

2.4.2 Bias circuit

Fig.7 shows the bias circuit for the symmetric load circuit. This circuit generates the voltage, V_{bias} which is the gate voltage of symmetric load. V_{bias} controls the resistance of the load. The circuit uses a positive feedback structure, providing transistor P_4 with a variable gate voltage which enables V_{bias} to track with the change of V_{ctrl} quickly. The bias circuit adopts the self-cascode structure which could offer the proper and stable bias voltage.[3]

2.4.3 Buffer stage(Full-swing amplifier)

The waveform of the VCO output is close to a sine waveform, but its output swing is small, so it needs wave shaping before applying to digital circuit. We adopt a buffer stage(Full-swing Amplifier) as the wave shaping circuit as shown in Fig.8. An active current mirror is used as input stage, which serves as a differential to single-ended converter and an amplifier. The inverter is designed to get rail-to-rail signal swing.[2]

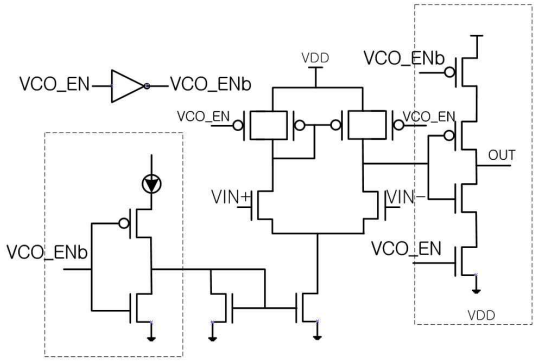


Fig.8. Proposed buffer stage circuit

2.5 Divider circuit

The divider circuit is composed of the divide-by-4 circuit and the dual-modulus 2/3 prescaler circuit.

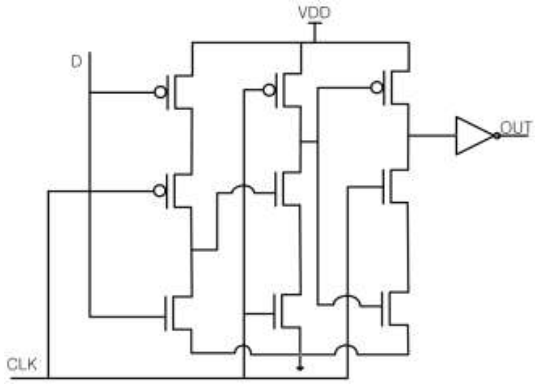


Fig.9. TSPC D flip-flop

The divide-by-4 circuit consist of two T flip-flops which are made of the TSPC D flip-flop. The schematic of TSPC D flip-flop is shown in Fig.9. The dual-modulus 2/3 prescaler circuit is designed by two D flip-flop, a AND gate and an OR gate. When the mode signal is 1 or 0, the CLK signal will be divide by 2 or 3 through the divider circuit. The control mode signal is provided by SDM(Sigma Delta Modulator) circuit, we use the external SDM circuit instead of including SDM circuit in this paper.

3.The simulation results

We use 0.18um CMOS process with 1.8V supply voltage to design a frequency synthesizer. Cadence Spectre tool is used for the circuit simulation of frequency synthesizer.

Fig.10 is the simulation result of the dual-modulus 2/3 prescaler circuit. From the result, the frequency is divided by 2 and divided by 3 alternately according to control signal. As a result, the frequency is divided by

2.5 in average.

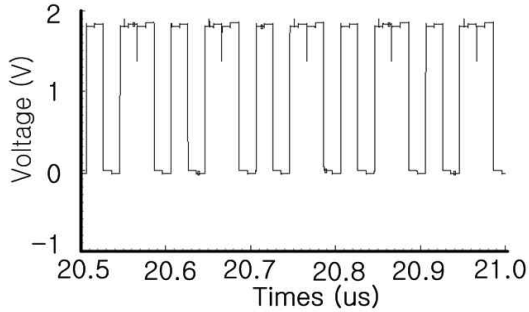


Fig.10. The result of Dual-Modulus 2/3 prescaler circuit

The locking result of 160MHz and 240MHz output frequency of VCO are shown in Fig.11 and Fig.12. Locking time is 23.8us and 20.7us respectively.

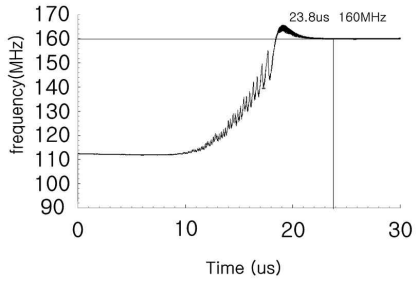


Fig.11. 160MHz locking result

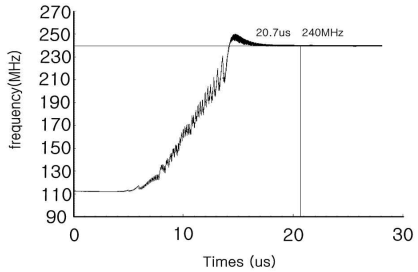


Fig.12. 240MHz locking result

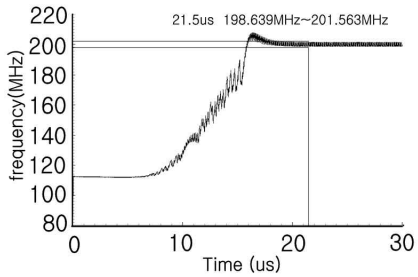


Fig.13. 200MHz locking result

The 200MHz output frequency which is the center frequency of AT-DMB is shown in Fig.13. The results show that the locking time is 21.5us, meanwhile, the output frequency jitter of VCO is about 1.5MHz. But jitter could be minimized by changing loop filter bandwidth.

Conclusion

This paper shows the frequency synthesizer using 0.18um CMOS process with 1.8V supply voltage for AT-DMB applications. The whole circuit is designed using Cadence Spectre tool and verified by it. The 7 stage ring oscillator is used to for VCO, and its tuning range is from 110MHz to 522MHz and satisfy AT-DMB specification. In the design of VCO, we used the modified symmetric load which has a good linearity in frequency and wide frequency range.

The simulation results of frequency synthesizer show that the locking time is 21.5us, and the output frequency of VCO is 198.639MHz ~ 201.563MHz. The 20MHz frequency is used to the reference frequency. This frequency synthesizer is suitable for AT-DMB applications. And this work could be extended other communication systems which have the similar frequency range.

Acknowledgments

This work was sponsored by KCC/ETRI, Source Technique Development Project for MicroWave Broadcasting Satellite.

REFERENCES

[1] Won-Hyo Lee; Jun-Dong Cho; sung-Dae Lee, “A High Speed and Low Power Phase-Frequency Detector and Charge-Pump”, Design Automation Conference pp.269-272vol.1,1999.

[2] Tuan-Vu Cao; Wisland,D.T Lande,T.s; Moradi,F, “Low-Voltage, Low-power, and wide-Tuning-Range Ring-VCO for Frequency ΔΣ Modulator,” NORCHIP, pp.79-84,2008.

[3] Honghui Deng; Yongsheng Yin; Gaoming Du, “Phase noise analysis and design of CMOS differential Ring VCO”, International Conference on electronic Measurement & Instruments, pp.4-731-4-736,2009.