A Study on Wide-band Frequency Synthesizer for Advanced Wireless Communication

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Abstract – A wide-band frequency synthesizer for advanced wireless communication including LTE(Long Term Evolution) is proposed. Inductor switching techniques and 4-bit capacitor bank are used in LC-VCO for wide frequency band, and varactor bank in LC-VCO is designed for low VCO-gain variation and uniform VCO frequency interval. Additionally, the output frequency can be selected by output-selection bits in the prescaler for choosing needed frequency. The proposed frequency synthesizer is designed by 0.18 \mu m CMOS process and occupies 0.21 mm². The simulated phase noise of VCO output is below -105dBc/Hz at 1MHz offset. The frequency synthesizer consumes 32.4 mW by 1.8V supply.

Keywords : Wide-band frequency synthesizer , VCO , phase locked loop(PLL) , LTE(Long Term Evolution)

I. INTRODUCTION

Advanced wireless communication like LTE has been introduced recently. Accordingly, semiconductor chipsets for mobile system are urgent to be developed because different LTE frequencies are used in each country. Therefore, semiconductor technology has been developed for integrating various systems for each country into one SoC. In addition to this requirement, it is important that system should be designed for low power dissipation, small chip size and high performance per cost. Especially, frequency synthesizer is key block for the performance of system. If frequency synthesizer satisfies wide frequency band and occupies small area, the system cost and size of communication system could be improved.

In this paper, frequency synthesizer is integrated using 0.18 \mu m CMOS process with 1.8 V supply. Inductor Switching techniques and 4-bit capacitor bank are used in LC-VCO for wide frequency band. The output frequency band could be selected by output-selection bits in the prescaler. Also, VCO gain is below 53MHz/V for low phase noise and varactor bank in LC-VCO is designed for minimizing VCO gain variation. The tuning range of the designed frequency synthesizer is 3.17GHz to 3.82GHz and 4.12GHz to 5.06GHz according to inductor switching status, which satisfies the requirements of the LTE, WiMAX and WiBro transceiver as summarized in Table 1. WiMAX band is supported by VCO output directly. WiBro and LTE bands are supported by the divided output of VCO.

Table 1. Frequency specifications for wireless communication

<table>
<thead>
<tr>
<th></th>
<th>Frequency band [MHz]</th>
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<tr>
<td>WiBro</td>
<td>2300</td>
</tr>
<tr>
<td>WiMAX</td>
<td>3400–3600</td>
</tr>
<tr>
<td>LTE</td>
<td>860, 880, 1500–2000, 2100</td>
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</table>

This paper is organized as follows. In Section II, the proposed frequency synthesizer structure and frequency characteristic are described. Design techniques for supporting wide frequency band are introduced in Section III, and simulation and measurement results follow in Section IV and V.

II. FREQUENCY SYNTHESIZER ARCHITECTURE

Figure 1. Block diagram of the wide-band PLL

The block diagram of the proposed wide-band PLL is illustrated in Figure 1. The PLL consists of PFD (Phase Frequency Detector), CP (Charge Pump), LF (Loop filter), wide-band VCO, prescaler and main divider.

The integrated VCO has 32 frequency curves by using 4-bit switched capacitor bank and 1-bit inductor switch. Also, 1-bit varactor bank is used in VCO, which is controlled by MSB of capacitor bank selection bits. It achieves reduced VCO phase noise as well as wide frequency band. The divider consists of prescaler and main divider. The prescaler is SCL type and determines PLL output frequency at high frequency operation of VCO. Main divider is programmable counter type divider with 6-bit control.

Inductor and capacitor switching technique is used to cover wide frequency band of about 1590MHz with small VCO gain at the supply voltage of 1.8 V. The frequency tuning range of VCO is 3.17GHz ~ 3.82GHz and 4.12GHz ~ 5.06GHz according to inductor switching status, which satisfies the requirements of the LTE, WiMAX and WiBro transceiver as summarized in Table 1. WiMAX band is supported by VCO output directly. WiBro and LTE bands are supported by the divided output of VCO.
III. Techniques for Supporting Wide-band

For supporting wide-band, SCL (Source Coupled Logic) type 4-to-1 MUX are used to choose the desired frequency in the prescaler and multi-band VCO is used in the proposed PLL.

A. Wide and Multi-band VCO Design

Figure 2 shows the schematic of the proposed LC VCO.

![Figure 2. The proposed multi-band LC VCO](image)

NP-core is chosen for VCO core to improve the symmetrical characteristic of output waveform and has low power dissipation. The proposed VCO uses inductor switching, capacitor bank and varactor bank for supporting wide frequency band. Multi-band frequency is generated by 4-bit capacitor bank, and thereby Kvco(VCO voltage gain) is lowered, so the fluctuation of oscillation frequency (fVCO) is minimized by the fine control of VCO control voltage(VCTRL).[1] The linearity and uniformity of the frequency-voltage gain characteristics can be deteriorated as oscillation frequency range is increased, because capacitance variation which is described is equation (1).[2] For compensating the decrease of Kvco and linearity, PMOS-varactor bank is used.

\[
\nu_t = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{(L_1 + L_2)(C_{var} + C_{capbank} + C_{parasitic})}}
\]

C_{var} : Capacitance of varactor bank
C_{capbank} : Unit capacitance of capacitor bank
C_{parasitic} : Parasitic capacitance

B. Divider Design

Figure 3 shows the structure of divider. Divider consists of a main divider and a prescaler. The PLL output frequency is selected among VCO output frequency passed through analog buffer, divided by 2 output frequency and divided by 4 output frequency according to 2-bit frequency band selection. Also, the prescaler is designed by TSPC (True Single Phase Clocking) D Flip-Flop and SCL MUX for operating in high frequency band. The main divider is programmable divider, which divides frequency by 1–64 according to 6-bit digital input.

![Figure 3. The structure of divider](image)

C. Inductor Design

Inductor Switching in the proposed VCO could control total inductance for supporting wide-band. Inductor size is important to decide VCO size. If two inductors are designed by in one inductor area, it has the merits of small area and low current consumption.[3] Figure 4.(a) shows general two symmetric inductors layout and figure 4.(b) shows the proposed inductor layout.

![Figure 4. (a) General two symmetric inductors layout (b) The proposed inductor layout](image)
The proposed symmetric inductor changes its total inductance by turning on or off the switch. The proposed inductor achieves about 27% smaller inductor size than general two symmetric inductors. Also current consumption is reduced from 2.2mA to 1.8mA with 1.8 V supply voltage because of parasitic effect reduction.

IV. SIMULATION RESULTS

Simulations are carried out using 0.18 μm CMOS technology. SPECTRE and HSPICE is used to verify the proposed frequency synthesizer.

A. VCO gain characteristics

Figure 5 shows the VCO gain characteristics according to VCO control voltage. We verified the output frequency of 3.17 GHz - 3.82 GHz and 4.12 GHz - 5.06 GHz.

B. Phase Noise

Figure 6 shows the simulation result of the phase noise according to target frequencies which are 3.2 GHz, 3.6GHz, 4.2 GHz and 4.6 GHz. VCO phase noise is lower than -105 dBc/Hz at 1 MHz offset at target frequencies.

C. Locking simulation results

Figure 7 shows the VCO control voltage when the PLL completes frequency generation. Figure 7.(a) shows the VCO control voltage in 860 MHz output frequency when inductor switch is opened and the oscillation frequency of VCO is 3440 MHz. Figure 7.(b) shows the VCO control voltage in 2.1 GHz output frequency when inductor switch is closed and oscillation frequency of VCO is 4.2GHz.

Figure 8 shows the layout of the proposed PLL without loop filter, which occupies the area of 330 μm x 620 μm excluding the pad area. The VCO layout is arranged as symmetrical as possible and all capacitors and transistors are placed nearby, so energy loss due to connecting wires could be minimized. The summary of the characteristic is given in Table 2. The proposed frequency synthesizer consumes 32.4 mW at 860 MHz output frequency.

Table 2. Performance Summary

<table>
<thead>
<tr>
<th>Process</th>
<th>0.18μm 1P9M CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply</td>
<td>1.8V</td>
</tr>
<tr>
<td>VCO Architecture</td>
<td>NMOS &amp; PMOS Cross Pair</td>
</tr>
<tr>
<td>Tuning words</td>
<td>13bits</td>
</tr>
<tr>
<td>VCO Freq. Tuning range</td>
<td>3.17 GHz ~ 3.82 GHz, 4.12 GHz ~ 5.06 GHz</td>
</tr>
<tr>
<td>Phase Noise(dBc/Hz)</td>
<td>-105.3dBc/Hz ~ -121.8dBc/Hz @ 1MHz</td>
</tr>
<tr>
<td>VCO Consumed Current</td>
<td>7.58 mA ~ 8.17 mA</td>
</tr>
<tr>
<td>Charge Pump</td>
<td>30 μA ~ 40 μA</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>20 kHz ~ 125 kHz</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>32.4 mW at 860MHz</td>
</tr>
</tbody>
</table>
V. MEASUREMENT RESULTS

The proposed chip is fabricated using 0.18 μm CMOS process and the layout of designed chip is shown in Figure 9.(a). The total chip area including pad, ESD circuit, decoupling capacitor and designed circuits is 4.5 mm x 4 mm. Figure 9.(b) shows the test board of the proposed frequency synthesizer.

![Figure 9. (a) The layout of the designed chip](image1)
![Figure 9. (b) The test board for the designed chip](image2)

Figure 10 shows experimental results of output frequency using spectrum analyzer. Figure 10.(a) shows the output power in 880 MHz which is the output frequency divided by 4 when inductor switch is opened. The output power is measured -28 dBm. Figure 10.(b) shows the output power in 1.6 GHz which is the output frequency divided by 2 when inductor switch is opened. The output power is measured -39.67 dBm. The proposed chip is fabricated using standard CMOS process, not RF process, so RF PAD is not used in chip design. So the PAD capacitance is somewhat large. Therefore, output power is lower than pre-simulation results using SPECTRE.

![Figure 10. (a) Experimental results in 880 MHz](image3)
![Figure 10. (b) Experimental results in 1.6 GHz](image4)

Figure 11 shows experimental results about VCO frequency characteristics according to VCO control voltage and gain distribution when inductor switch is opened. As shown in figure 11.(a) the output frequency divided by 4 is measured 774.4 MHz -920.7 MHz. These results satisfy LTE specification.

![Figure 11. (a) VCO frequency characteristics](image5)
![Figure 11. (b) VCO gain distribution](image6)

Figure 11.(b) shows experimental results about VCO gain distribution. The VCO gain is measured 18.93 MHz/V – 26.56 MHz/V. These results are lower than pre-simulation results due to parasitic capacitance, which is 27.09 MHz /V - 36.25 MHz/V.

VI. CONCLUSIONS

In this paper, the integrated wide-band frequency synthesizer for advanced mobile communication is designed using 0.18 μm CMOS process with 1.8V supply. Wide-band VCO is designed by inductor switching, capacitor-bank and varactor-bank complements the decrease of Kvco for supporting wide-frequency band. The designed frequency synthesizer consumes 32.4 mW at 860 MHz output frequency from single 1.8 V supply voltage and VCO phase noise is lower than -105 dBc/Hz at 1MHz offset for 800 MHz, 900 MHz, 2.1 GHz and 2.3 GHz. The VCO tuning range is as wide as 1590 MHz from 3.17 GHz to 3.82 GHz and from 4.12 GHz to 5.06 GHz in 32 channels, which can cover all the desired frequencies for LTE, WiMAX and WiBro specifications. The proposed inductor in VCO achieves about 27% smaller inductor size than general two symmetric inductors. Also current consumption is reduced from 2.2mA to 1.8mA with 1.8 V supply voltage. CAD tools and MPW is supported by IDEC. This work could be useful to implement wide-band PLL applications for advanced communication.

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