# A W-band VCO using center-tapped basic inductor in 65nm CMOS

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**Abstract**

A W-band voltage controlled oscillator (VCO) is implemented using 65nm CMOS process. The proposed VCO uses center-tapped inductor modified from basic structure and has high Q-factor. Inductor based LC type topology has many advantages compared with transmission line or waveguide. Also low cost CMOS process has many advantages than other processes. The designed VCO operates at 77.52~79.33GHz. The phase noise at 1MHz and 10MHz offset of 78GHz carrier are -81.6dBc/Hz and -102dBc/Hz respectively. Supply voltage is 0.9V and power consumption is 2.97mW. The chip area is 0.12x0.20mm$^2$ and output power is -20.04dBm. Calculated FOM is -175.27dB.

***Keywords-CMOS, voltage controlled oscillator (VCO), W-band, waveguide, transmisson line***

## I. INTRODUCTION

For High speed data transmission, the demand of monolithic microwave integrated circuits (MMIC) is increasing such as wireless LANs . A voltage controlled oscillator (VCO) is an inevitable component for data transmission system [1-4]. VCO in W-band is mostly implemented by InP HBT, DHBT, SiGe HBTs, HEMT and BiCMOS for high frequency operation [5-7]. However, these processes have drawbacks of high cost and high power consumption. So research of CMOS technology is ongoing and CMOS VCO in deep-submicron technology enables VCO to operate at W-band. In W-band, VCO mainly uses transmission line or waveguide based inductor for low inductance. However, an inductor-based LC type resonator is used favorably compared with other types. Inductors designed using waveguide or transmission line have the advantage of high characteristic impedance [2]. High characteristic impedance requires lower $g_m$, so it can reduce size of transistor. Small transistors go with cause low parasitic capacitance and low power consumption. This work demonstrates CMOS VCO has better FOM than previous VCO's and planar inductor, not transmission line or waveguide, is used for LC resonator in W-band. And the proposed VCO uses center-tapped basic inductor which shows has better performance than other CMOS VCO's.

## II. VCO ARCHITECTURE AND CIRCUIT DESIGN

The proposed VCO is designed similarly according to previous work [3] which is basic cross-coupled differential LC type VCO. The reason that we adapted the cross-coupled pair of MN1 and MN2 is to ensure the differential mode operation and to compensate losses from the passive components. Additionally, as the surface mobility of PMOS transistors is more slow than that of NMOS, and NMOS core is suitable for operation at high frequency. PMOS transistors are used in the bias circuit to reduce the flicker noise for better phase noise performance. However, due to the lack of high-Q on-chip passive components such as inductor, VCO suffers from poor phase noise in high frequencies. So we used center-tapped inductor topology to have higher inductor Q-factor and the advantage of chip area. The schematic of proposed VCO is shown in Fig. 1.

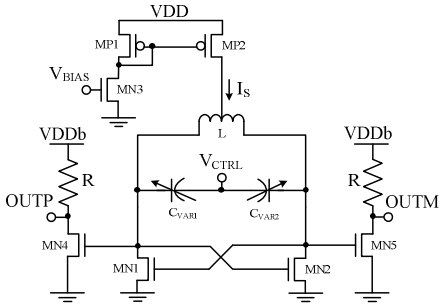



Fig. 1 Proposed VCO schematic

Proposed VCO has output buffer including 50Ω -matching network and power supply separation structure to prevent noise increase. In order to realize mm-wave frequencies, the values of the inductance and capacitance should be small, because the oscillation frequency of VCO is decided by these values. The oscillation frequency formula with parasitic elements is described in equation 1.

$$Frequency = \frac{1}{2\pi\sqrt{\frac{L}{2}(Cvar1 + Cbuff + CNM + Cpar)}} \quad (1)$$

In equation (1), $L$ is the value of the inductor in VCO, $C_{var1}$ (= $C_{var2}$) is the capacitance of varactor, and $C_{buff}$ is the input capacitance of the output buffer. $C_{NM}$ is the capacitance looking at the drain of the cross-coupled NMOS such as $C_{DS}$ and $C_{DB}$ of MN1 and MN2. $C_{par}$ is the capacitance distributed along the connecting metal lines. The smaller values of the inductor and capacitor are essential for the design of W-band VCO, as we see in equation 1. In this point of view, NMOS has an advantage over PMOS because the size of NMOS is smaller than PMOS.

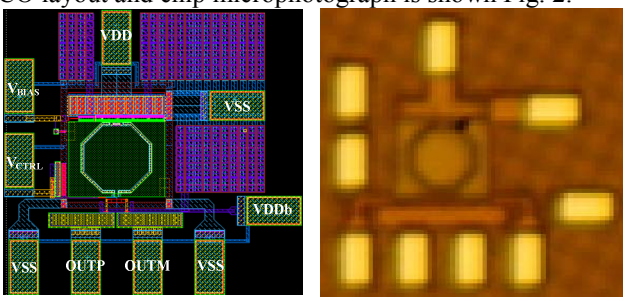
In order to widen Frequency Tuning Range (FTR), we optimize varactor tuning voltage ($V_{CTRL}$) and bias voltage ($V_{BIAS}$). As a result, we get 2.3% FTR from simulation result. FOM equation is shown in equation 2.

$$FOM = L\{\Delta f\} - 20log\left(\frac{f0}{\Delta f}\right) + 10log\left(\frac{P_{DC}}{1mW}\right) \qquad (2)$$

In equation 2, $P_{DC}$ is the power consumption and smaller $FOM_T$ means the better performance of the VCO.

## III. IMPLEMENTATION AND POST SIMULATION RESULTS

The designed VCO was implemented by 65nm CMOS process and verified from cadence spectre simulator. Simulation results of cadence spectre compared with the measurements are generally accurate to within 5% [2]. The VCO layout and chip microphotograph is shown Fig. 2.




(a) (b)

Fig. 2. (a) VCO layout (b) Chip micrograph

Fig. 3 shows frequency tuning range and output voltage swing versus $V_{CTRL}$ when $V_{BIAS}$ is 0.4V and 0.9V respectively.

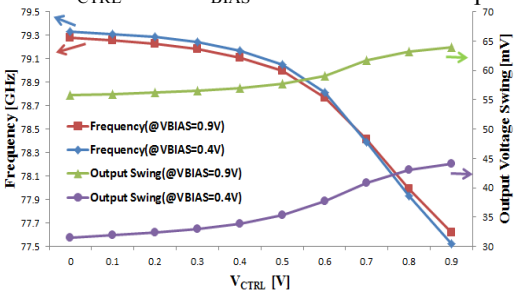



Fig. 3. The oscillation frequency and output voltage swing

Fig. 4 shows the output power and power consumption versus $V_{CTRL}$. The FTR is from 77.52 to 79.33GHz, and the output power is between -20.16 and -21.10 dBm while the $V_{CTRL}$ is between 0 and 0.9V.

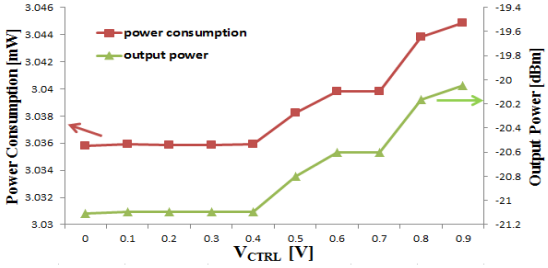



Fig. 4. The output power and output voltage swing

The phase noise at 1MHz and 10MHz offset of the 78GHz carrier are -81.6dBc/Hz and -102dBc/Hz respectively and it is shown Fig. 5.

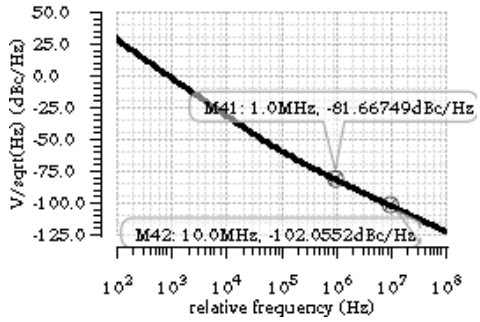



Fig. 5. Phase noise of VCO at center frequency

In order to predict chip performance, it is important to verify the process variation. So we have changed model library parameters of NMOS and PMOS, and the additional results of corner simulation with slow-slow(ss) and fast-fast(ff) models are obtained. Fig. 6 shows the frequency tuning range and output voltage swing versus $V_{CTRL}$.

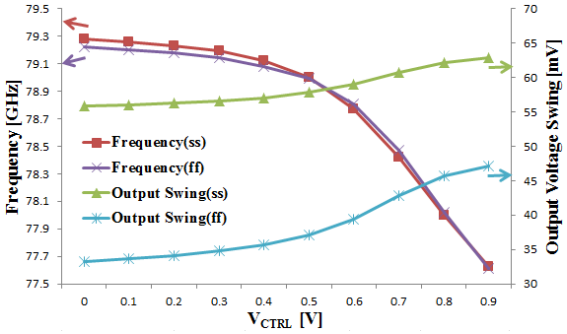



Fig. 6. The corner simulation results

According to simulation results, proposed CMOS VCO has superior performance compare with existing VCO's which have W-band frequencies. TABLE I summarized the performance comparison between the proposed work and recently reported VCOs.

TABLE I. Performance and summary and comparisons

| | [5]RFIC 2013 | [4]LMWC 2012 | [6]MWSYM 2012 | [7]NWECAS 2011 | *This work |
|---|---|---|---|---|---|
| Process | 0.13um BiCMOS | 90nm CMOS | 50nm InP DHBT | 0.13um SiGe HBT | 65nm CMOS |
| Supply Voltage[V] | 1.5~2.7 | 1.4 | 4 | 1.8 | 0.9 |
| Frequency [GHz] | 73.9~ 83.5 | 79.32~ 82.09 | 77.11~ 78.39 | 77~ 81 | 77.52~ 79.33 |
| Phase Noise [dBc/Hz] | -88.5@100KHz -111@10MHz | -104.2@10MHz | -94@1MHz | -108@10MHz | -81.6@1MHz -102@10MHz |
| Output Power [dBm] | -4 | -26 | -21.5 | -16 | -20.04 |
| FOM[dB] | -170.86 | -173.7 | -172.6 | -165.51 | -175.27 |
| $P_{DC}$[mW] | 55 | 7.06 | 84 | 108 | 3.03 |

*Simulation result

## IV. CONCLUSION

A W-band CMOS VCO using center-tapped inductor is presented. The VCO topology is NMOS cross-coupled differential LC type using center-tapped inductor modified

from basic structure to derive high Q-factor. In order to obtain good phase noise performance, We focus on the design of inductor. Also, inductor based VCO has low power consumption compared with transmission line or waveguide. Inductor is designed by cadence spectre simulator and VCO performance is verified by post-simulation results. The designed VCO operates at 77.52~79.33GHz(2.3% FTR) and phase noise at 1MHz and 10MHz offset of the 78GHz carrier are -81.6dBc/Hz and -102dBc/Hz respectively. It is implemented by 65nm CMOS process and chip area is $0.12x0.20mm^2$. CMOS process is very low compared with other processes such as InP HBT, DHBT, SiGe HBTs, HEMT and BiCMOS. Post simulation shows that power supply voltage is 0.9V, power consumption is 2.97mW, and output power is -20.04dBm. And these value are verified by simulation results. Calculated FOM is -175.27dB. In this study, the proposed VCO is expected to be useful for high-speed data transmission.

## Acknowledgment

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