A Design of Low Power 70GHz CMOS VCO for Wireless Communication system

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***Abstract*—A 70GHz Voltage Controlled Oscillatior (VCO) for wireless communication system is proposed by 0.11㎛ CMOS process. The VCO is designed by a center-tapped spiral inductor and NMOS cross-coupled structure and includes output buffer. The designed VCO oscillates from 69.95 to 71.62GHz and this frequency band is proper to wireless communication system in cars. The measured output power is –22.9dBm and phase noise is –78.67dBc/Hz at 1MHz offset at 71.18GHz. The power consumption of the VCO core is only 2.6㎽ at the supply voltage of 1.2V. VCO shows good figure of merit (FOM) of –171.57dBc/Hz.**

***Keywords*— PLL(Phase Locked Loop), Wireless communication system, VCO(Voltage Controlled Oscillator), Center-tapped inductor, CMOS**

I. INTRODUCTION

Millimeter wave oscillator design on CMOS is required for low cost and low power consumption [1-4]. However, the use of CMOS at mm-Wave frequencies also accompanies lower transistor gain, larger parasitic components and poor passive components, compared to III-V technologies. To solve these problems, we used a spiral type inductor to reduce the required g_m of the transistor and to reduce parasitic components.

This paper introduces low power 70GHz VCO for wireless communication system and describes the measurement results of implemented VCO. And the paper summarizes the performances of the designed VCO and conclusions.

II. VCO ARCHITECTURE

The proposed VCO operates at 70GHz in V-band and adopts NMOS cross-coupled differential LC structure. And it reduces the loss of LC resonator because of negative resistance ($-2/g_m$). Fig. 1 describes the schematic of the proposed VCO. To minimize variation of elements and reduce parasitic component, VCO is designed with minimum elements. And it can reduce the power consumption of VCO. A VCO based on waveguide or transmission line is possible to oscillate at millimeter band, but it requires high power consumption and eventually leads to a large parasitic capacitance because the low resistance of output load requires high g_m of transistor.

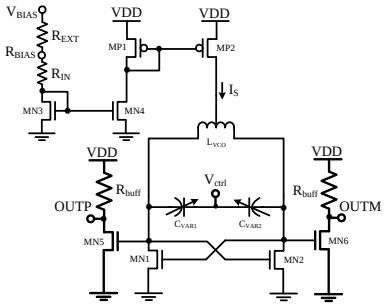


FIG. 1. VCO schematic

VCO based on inductor has lower g_m from transistor and leads to low power consumption and small parasitic capacitance because inductor provides very large impedance at the LC resonance frequency. Research on the inductance and shape of inductor was carried out because of limited values in width and diameter of the inductor given to the process. The optimized width and diameter with the highest Q-factor in 70GHz was selected from simulation. By adjusting the capacitance of varactor, V_{ctrl} changes output frequency. Additionally, V_{BIAS} and R_{EXT} are used for widening frequency tuning range by controlling I_S. R_{IN} is the internal resistor that could reduce unexpected damage to the circuit because an external signal input to the circuit could be limited by the resistor. Output buffer is added for impedance matching and isolation to the next stage.

III. MEASUREMENT RESULTS

The proposed VCO is implemented by 0.11㎛ CMOS process and Fig. 2 shows the chip photograph of the VCO and total area is $0.18\times0.26mm^2$. CADENCE Spectre RF is used for simulation verification and on-wafer probing was carried out using a probe station for measurement. Fig. 3 shows the simulation results. If R_{EXT} is small, I_S increases because the current of the first stage current source increases, which increases the drain current (V_{ds}) of cross-coupled NMOS. As V_{ds} of MN1 and MN2 increases, the voltage across the varactor is reduced and the capacitance is reduced, so the frequency of VCO is increased. Changing the R_{EXT} could generate the

frequencies of the desired band even if process, temperature and supply voltage variation exists.

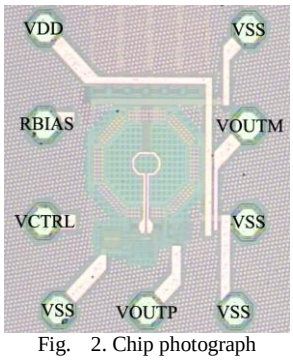


Fig. 2. Chip photograph

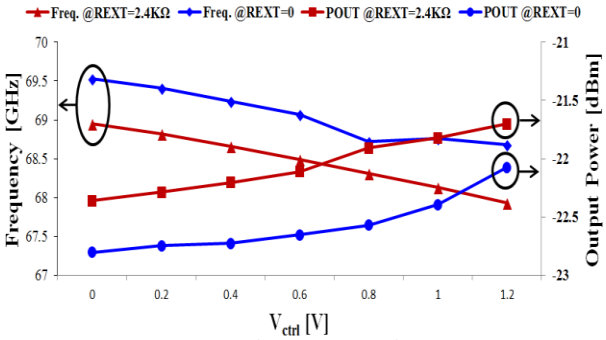
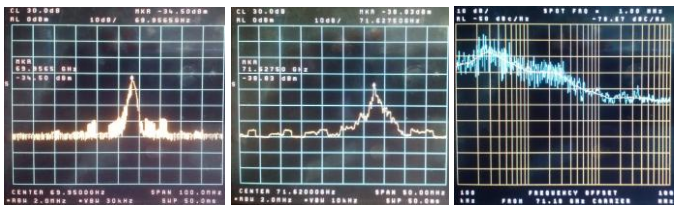


Fig. 3. Simulation results of the oscillation frequency and output power versus R_{EXT} and V_{ctrl}

Fig. 4. (a) and (b) show the results of spectral analysis of the output signal. Considering the cable loss of 1.1dB and the adaptor loss of 0.5dB between cable and spectrum analyzer, the output power is -22.90dBm at 69.95GHz and -27.23dBm at 71.62GHz respectively (ATTEN:10dB). Measured frequency tuning range of VCO is from 69.95 to 71.62GHz by changing V_{ctrl}, V_{BIAS} and R_{EXT}. The frequency goes up, the output voltage should be changed quickly, so the output power is low. The measured phase noise is -78.67dBc/Hz at 1MHz offset from carrier frequency of 71.18GHz and shown in Fig. 4. (c).



(a) (b) (c)

Fig. 4. Measured output power of VCO at (a) 69.95GHz (b) 71.62GHz And (c) measured phase noise of the VCO at 1MHz offset

For performance comparison with other VCOs, the following FOM characteristics equation (2) is used[1].

$$FOM = PN\{\Delta f\} - 20\log\left(\frac{f_0}{\Delta f}\right) + 10\log\left(\frac{P_{DC}}{1mW}\right) \quad (2)$$

Where PN{Δ f} is phase noise in dBc/Hz at the offset frequency of Δ f. P_{DC} is power consumption of VCO in mW. If FOM is smaller, it means that the performance is better. The FOM of the proposed VCO is -171.57dBc/Hz and shows superior performance to other VCOs in similar frequency band. And power consumption is excellent compared with other VCOs. In Table 1, the proposed VCO and existing VCO's performances are compared.

TABLE I. THE PERFORMANCE WITH PREVIOUS WORKS

	[2]COMCAS 2009	[3]RFIC 2011	[4]ISOCC 2012	this work
Process	**45nm CMOS**	**65nm CMOS**	**65nm CMOS**	**0.11㎛ CMOS**
Center Freq. [GHz]	**70**	**77**	**62.8**	**70**
Phase Noise [dBc/Hz]	**-100.02@10M**	**-88@1M**	**-107@10M**	**-78.67@1M**
FTR[%]	**0.2**	**14.5**	**13.9**	**2.4**
PDC[mW]	**45.6**	**190**	**15.5**	**2.6**
FOM [dBc/Hz]	**-160.33**	**-162.94**	**-171.06**	**-171.57**

IV. CONCLUSIONS

For the transmitter of wireless communication system, VCO was implemented by 0.11㎛ CMOS process. The architecture of the proposed VCO is NMOS cross coupled differential LC type with minimum elements to reduce process variation and power consumption. To widen frequency tuning range, V_{ctrl}, external resistor and bias voltage are used. The measured frequency tuning range is from 69.95 to 71.62GHz and output power is –22.9dBm. And the measured phase noise is –78.67dBc/Hz at 1MHz offset from 71.18GHz and power consumption of VCO core is only 2.6㎽ at supply voltage of 1.2V. The calculated FOM of the proposed VCO is –171.57dBc/Hz. CAD tool was supported by IDEC.

ACKNOWLEDGMENT

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