

And a current source is added for the VCO to widen frequency tuning range and we get good phase noise performance. Because the surface mobility of PMOS transistors is slower than that of NMOS, so PMOS transistors are used in the bias circuit to reduce the flicker noise for better phase noise performance. V_{BIAS} can control I_S , then I_S adjusts the oscillation frequency because the oscillation frequency depends on not only inductance and capacitance but also the resistance of the VCO. V_{CTRL} also changes the oscillation frequency by changing the capacitance of varactor. R_{IN} is the internal resistor that could protect unexpected damage to the circuit because an external input signal current to the circuit in automobile circumstance could be limited by the resistor.

A VCO based on waveguide or transmission line is possible to oscillate at W-band, but it requires high power consumption and eventually leads to large parasitic capacitance because the low resistance of output load requires high g_m of transistor. So we used native inductor layer structure with modified shape by using simulator. Research on inductance and capacitance with the shape of inductor was carried out because of limited values in width and diameter of the inductor given by the process. The optimized width and diameter with highest Q-factor in 77~79GHz were selected from simulation. We use upper two metal layers in inductor layout to guarantee the skin depth of metal at high frequency. For high output swing, two pairs of the inductors have mutual inductance by placing each other closely. And this layout technique also results in area reduction. The output buffer is added for 50Ω impedance matching and isolation to the next stage. The schematic of output buffer is shown in Fig. 2.

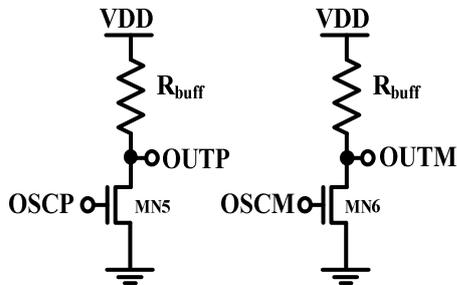


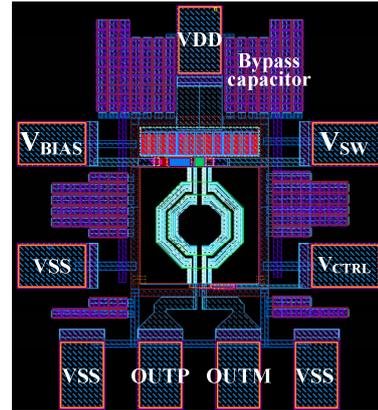
Fig. 2. Schematic of output buffer

If the sizes of MN5 and MN6 are large, OUTP and OUTM have larger swing but the operating frequency goes down. This is because MN5 and MN6 have to pass high current. Otherwise in order to get high operating frequency, the parasitic capacitances of the VCO should be minimized and the switching role of transistor is more important. So the sizing of MN5 and MN6 should be very careful to trade between the large output swing and high operating frequency. We use low-

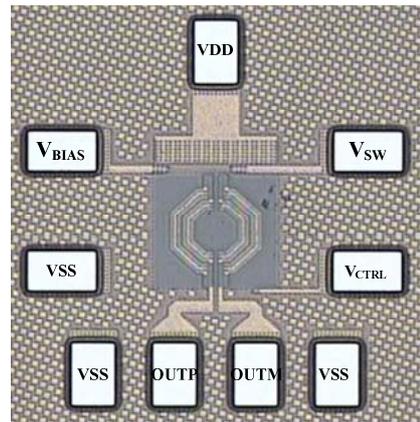
V_t NMOS transistor for high operating frequency and large output swing is obtained by high input swing (OSCP and OSCM) from the inductors connected to MN1 and MN2.

III. POST-SIMULATION RESULTS

The proposed dual-band VCO is implemented by 65nm CMOS process and Fig. 3 shows the chip layout and microphotograph of the VCO. The area is $0.15 \times 0.21 \text{mm}^2$ and CADENCE Spectre RF is used for simulation.



(a)



(b)

Fig. 3. (a) Layout of VCO (b) Die microphotograph

The simulation is accomplished by the post-layout parameters and similar measurement environment. Fig. 4 shows the simulation results of the output frequency versus V_{CTRL} and V_{BIAS} . If V_{SW} is 1.2V, NM3 is ON as switch and the output frequency is decreased because the capacitance between drain and source of NM3 is bigger than C_{VAR} . On the contrary, If V_{SW} is 0V, C_{VAR} does not affect the operation frequency. This is because the capacitance of drain and source of MN3 and C_{VAR} are connected in series. So the output frequency increases. We designed the VCO for two bands, 77GHz and

79GHz, and K_{VCO} is 0.67GHz/V and 1.5GHz/V, respectively. Additionally V_{BIAS} could widen the tuning range of the VCO by controlling I_S and shown in Fig. 4.(b).

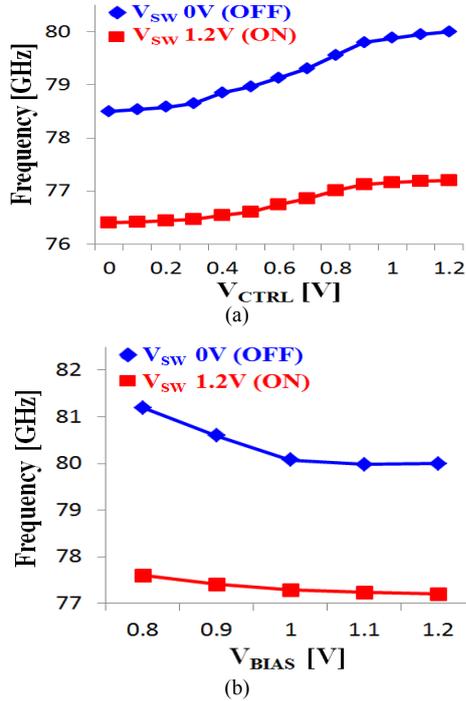


Fig. 4. Simulation results of the frequency versus (a) V_{CTRL} and (b) V_{BIAS}

If V_{SW} is 1.2V, the drains of NM1 and NM2 are short from DC point of view. So the resistance between NM1 and NM2 is low. This leads to low output swing. These simulation results are shown in Fig. 5. If V_{SW} is 0V, the drains of NM1 and NM2 are split and the capacitance between drain and source of MN3, C_{SW} , is remained [5]. Then, C_{VAR} and C_{SW} seem like series and the total capacitance is smaller than C_{SW} because C_{VAR} is larger than C_{SW} [5]. The operating frequency increases because the capacitance of LC resonator of the VCO is lower.

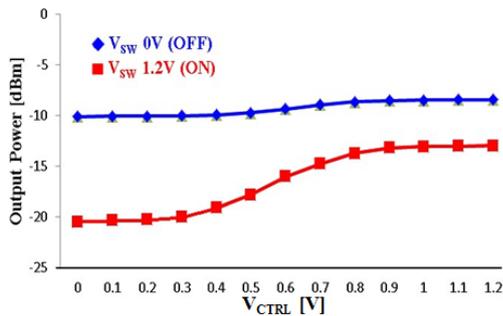


Fig. 5. Output power of the VCO

The maximum output power of the VCO is about -8.4dBm

when MN3 is OFF and V_{CTRL} is 1.2V. And the phase noise is -90.8dBc/Hz at 1MHz offset and -113.3dBc/Hz at 10MHz offset and shown in Fig. 6.

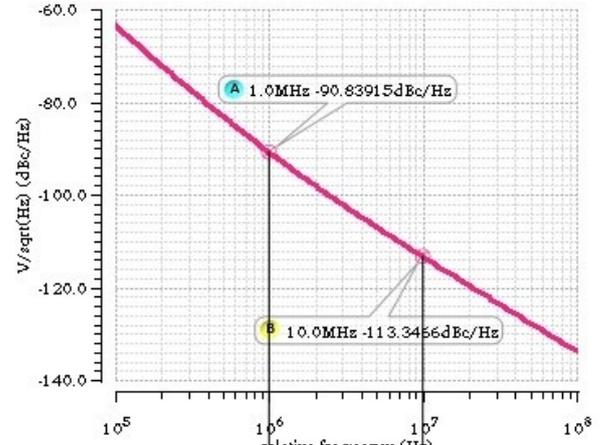


Fig. 6. Phase noise of the VCO

For the performance comparison with other VCO's, the following FOM characteristics equation (1) is used.

$$FOM = PN\{\Delta f\} - 20\log\left(\frac{f_0}{\Delta f}\right) + 10\log\left(\frac{P_{DC}}{1mW}\right) \quad (1)$$

Where $PN\{\Delta f\}$ is phase noise in dBc/Hz at the offset frequency of Δf . P_{DC} is the power consumption of the VCO in mW. If FOM is smaller, it means that the performance of the VCO is better. The FOM of the proposed dual-band VCO is -176.6dBc/Hz and shows superior performance to other VCO's in similar frequency band and process. And the phase noise from small K_{VCO} is excellent compared with other VCO's. In Table 1, the performance of the proposed VCO and previous VCO's are summarized.

TABLE I. THE PERFORMANCE COMPARISON WITH PREVIOUS WORKS

	[1]ISOC 2011	[2]RFIC 2011	[5]ISSC 2013	*this work
Process	65nm CMOS	65nm CMOS	32nm CMOS	65nm CMOS
Tuning Range [GHz]	69.6~81	77~81	33.6~46.2	ON:76.4~77.2 OFF:78.5~80
Phase Noise [dBc/Hz]	*-85@1M	-88@1M	-118@10M	-90.8@1M -113.3@10M
Output Power [dBm]	*-5	6	N/A	-8.4
P_{DC} [mW]	*100	190	9.8	30
FOM [dBc/Hz]	-163	-162.9	-178.4	-176.6

*Simulation Results

IV. CONCLUSIONS

For the automotive radar system, the dual-band VCO at W-band was proposed by 65nm CMOS process. The architecture of the proposed VCO is NMOS cross coupled differential LC type with splitting inductor for high frequency inductor tuning. So the proposed VCO operate at 77GHz long-range and 79GHz short-range radar sensor system. Low K_{VCO} design and the PMOS current source are used to obtain good performance of phase noise. Also the PMOS current source widens the tuning range of the VCO by controlling the current of the VCO. The post-simulation results show that the precise dual-band operation from inductor tuning split technique. The output power is -8.4dBm and the phase noise are -90.8dBc/Hz at 1MHz and -113.3dBc/Hz at 10MHz offset. The power consumption of the VCO is 30mW at the supply voltage of 1.2V. The VCO shows good FOM of -176.6dBc/Hz . So the proposed VCO shows superior performance to other VCO's in similar frequency band and process.

This work enables high performance frequency synthesizer as realization of automotive radar. The frequency synthesizer

using the proposed VCO will form the basis for automotive radar development. CAD tools are supported by IDEC.

REFERENCES

- [1] Joonhong Park, Hyuk Ryu and Donghyun Baek, "77 GHz signal generator with CMOS technology for automotive radar application," International SoC Design Conference, IEEE, pp.444-445, Nov. 2011.
- [2] Vishal P. Trivedi, Kun-Hin To and W.Margaret Huang, "A 77GHz CMOS VCO with 11.3GHz Tuning Range, 6dBm Output Power, and Competitive Phase Noise in 65nm Bulk CMOS," Radio Frequency Integrated Circuits Symposium, IEEE, pp.1-4, Jun. 2011.
- [3] FD W. Ying, P. Qin, J. Jin, and T. Mo, "A 1mW 5GHz current reuse CMOS VCO with low phase noise and balanced differential outputs," Integrated Circuits (ISIC), 13th International Symposium on Components, Circuits, Devices & Systems, pp. 543-546, Dec. 2011.
- [4] Huang Wang, Ling ling Sun, Jun Liu, Jincai Wen and Zhiping Yu, "Transfer Function Analysis for Model Topology Determination of On-Chip Transmission Lines," Integrated Circuits (ISIC), 13th International Symposium on Components, Circuits, Devices & Systems, pp. 273-276, Dec. 2011.
- [5] E. Mammei, E. Monaco, A. and F. Svelto, "A 33.6-to-46.2GHz 32nm CMOS VCO with 177.5dBc/Hz minimum noise FOM using inductor splitting for tuning extension," ISSCC, IEEE, pp.350-351, Feb. 2013.