A U-band VCO in 65nm CMOS with 0.44dBm output power

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Abstract

A high output power VCO (voltage controlled oscillator) in U-band is implemented using 65nm CMOS process. The proposed VCO uses MTM(meta-material) technique with transmission line to increase output voltage swing and overcome the limitation of the CMOS technologies. Two varactor banks widen frequency tuning range upto 5%. The VCO operates at 51.55~54.18GHz and the measured phase noise is -100.67dBc/Hz at 10MHz offset. The chip area is 0.16x0.16mm^2 and the output power is 0.44dBm. The power consumption is 33.6mW with 1.2V supply voltage. The measured FOM_P is -181dBc/Hz.

Keywords-CMOS, voltage controlled oscillator (VCO), U-band, transformer, transmisson line

I. Introduction

VCO is an inevitable component to implement a single-chip radio in communication system [1]. But CMOS VCO has the limitation of low Q-factor in on-chip passive components [2-3]. So transformer feedback technique is used to increase the output voltage swing, and transmission line theory is used to get the inductance of LC resonator enhance the high frequency performance [1-4]. The high output power could correctly transfer data but deteriorates phase noise performance. The frequency tuning range of VCO is also important factor and the capacitance value of LC resonator decides the tuning range of VCO in U-band [3]. So the proposed VCO uses two varactor banks to widen tuning range.

The remainder of this paper is organized as follows. In Section II, the proposed transformer VCO topology and the circuit design are presented. The circuit implementation and experimental results of VCO are provided in Section III. Finally, the conclusion is given in Section IV.

II. VCO Architecture and Circuit Design

The proposed VCO architecture is NMOS cross-coupled pair differential LC type and the transformer inductors using MTM concept are spiraled by L_{P1}, L_{P2} and L_{S1}, L_{S2} as shown in Fig. 1. The transformer inductors can provide drain-to-source feedback and voltage swing below ground. The two varactor banks, C_{VAR1} and C_{VAR2}, are used to widen tuning range of VCO. The value of C_{VAR1} is twice that of C_{VAR2}. The output buffers, MN3 and MN4, are added to isolate the output of VCO from other block but output swing is reduced somewhat. And the output buffer includes 50Ω- matching network.

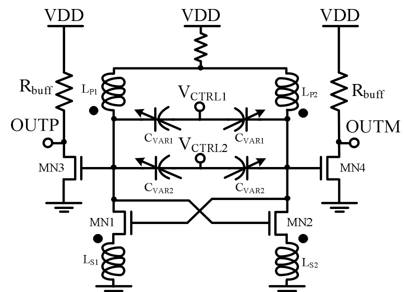

Fig. 1 Proposed VCO schematic

The cross-coupled pair of MN1 and MN2 ensures the differential mode operation and compensates loss from the passive components. The size of MN1 and MN2 is decided to sufficient gain for oscillating condition and better phase noise performance. The negative resistance of cross-coupled pair cancels the positive resistance of LC tank for oscillation. Additionally, as the mobility of PMOS transistors is lower than that of NMOS, so NMOS core is suitable for operation at high frequency.

III. Circuit Implementation and Experimental Results

The designed VCO was implemented by 65nm CMOS process and verified from cadence spectre RF simulator. The VCO chip microphotograph is shown in Fig. 2.

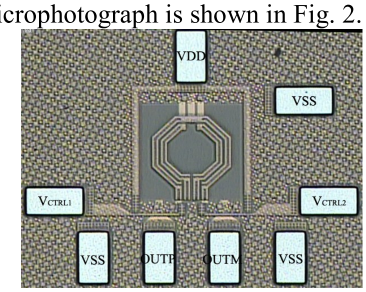

Fig. 2. VCO Chip micrograph

The four inductors are implemented by transmission line and L_{P1} (or L_{P2}) is placed close to L_{S1} (or L_{S2}) to get the high mutual inductance and high-Q. By doing this, we get the advantage in area and the area of VCO including buffer is only 0.16×0.16mm^2. The inductors in inner circle have wider width to get small inductance. L_{P1} and L_{P2} are placed at outer circle to have more inductance. We optimized the width and length of inductance to get output power as large as possible. If coupling coefficient K is 1, the output swing is shown in Eq. (1).

$$\text{Output swing} = \left(1 + \sqrt{\frac{L_P}{L_S}}\right) \bullet \text{VDD} \qquad (1)$$

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So the source inductor can swing below ground, on the other hand, if the value is too large, the oscillation is suppressed.

In measurement, on-wafer probing was carried out using a probe station, and N9010A spectrum analyzer, 11970V external mixer, N9029AE13 diplexer and dual power supply are used. Fig. 3 shows the measured frequency tuning range versus V_{CTRL1} and V_{CTRL2}.

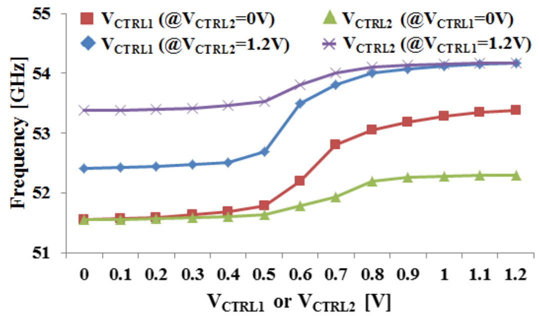
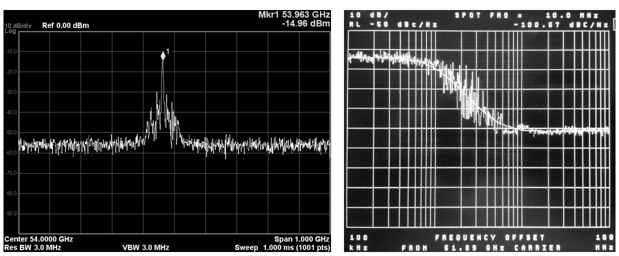


Fig. 3. The measured oscillating frequency of VCO

The FTR (Frequency Tuning Range) is from 51.55 to 54.18GHz, and the variation of V_{CTRL1} is larger than that of V_{CTRL2} as C_{VAR1} has more capacitance compared to C_{VAR2}. For the performance verification of VCO, the output power and phase noise are measured and shown in Fig. 4.



(a) (b)

Fig. 4. (a) Measured output power and (b) phase noise versus offset frequency

The losses of measurement environment exist and we compensate those and the values are as follows. 1.2dB at Probe, 2.2dB of two Cables, 0.5dB of Adapter and 1.5dB of Diplexer are given from datasheet. So the compensated output power is 0.44dBm (ATTEN:10dB) and which is very high output voltage swing in millimeter wave data transfer system. And the measured phase noise is -100.67dBc/Hz at 10MHz offset. By using these measured values, the proposed VCO are compared to other works to verify the performance. FOM_P is used for evaluation and defined as [4],

$$FOM_P = L(\Delta f) - 20\log(\frac{f_0}{\Delta f}) - \log(\frac{P_{RF}}{1mW}) - 10\log(\eta) \quad (2)$$

Where $L(\Delta f)$ is the phase noise, Δf is offset frequency, f_0 is the oscillation frequency, P_{RF} is RF output power and η is the dc-to-RF efficiency as

$$\eta = \frac{P_{RF}}{P_{DC}} \bullet 100\% \quad (3)$$

In equation (3), P_{DC} is DC power consumption. The proposed VCO shows superior performance compared with existing VCO's which uses the same technologies. TABLE I summarized the performance comparison between the proposed work and recently reported works.

TABLE I. Performance and summary and comparisons

	[1]RFIC 2012	[2]ESSCIRC 2012	[3] TCSI 2014	This work
Process	65nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS
Supply Voltage[V]	0.5	1.2	1	1.2
Operating Frequency[GHz]	37~44.1	48.8~62.3	57~65.5	51.55~54.18
Phase Noise [dBc/Hz]	-96@1MHz	-94@1MHz	-108.3@10MHz	-100.67@10MHz
Output Power[dBm]	-10	-43	-20.97	0.44
FOM_P[dBc/Hz]	-178	-163	-157	--181
P_{DC}[mW]	10	30	6	33.6

IV. CONCLUSION

A U-band 65nm CMOS MTM VCO having high output power and excellent FOM_P is designed. The VCO topology is NMOS cross-coupled pair differential LC type using transmission line and drain-to-source feedback structure for high output swing. The inductors are located close to each other to derive high Q-factor and large inductance. This structure has the advantage in area and the area of proposed VCO is $0.16\times0.16mm^2$. To widen tuning range, two varactor banks is used and the measured operating range is from 51.55 to 54.18GHz. The measured output power is 0.44dBm and phase noise is -100.67dBc/Hz at 10MHz offset. The power consumption is 33.6mW with 1.2V power supply and FOM_P is -181dBc/Hz which shows better performance than previous works. In this study, the proposed VCO is useful for millimeter wave data transfer systems. CAD tool and MPW was supported by IDEC.

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