A design of META-VCO based-on meta-material using CMOS process

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Abstract—**A low phase noise META-VCO applying meta-structure was designed using 65nm CMOS process. The META-VCO operates 8.45~8.77 GHz according to V_{CTRL}, and the output power is -19.12 dBm. The measured phase noises are -67.8 dBc/Hz, -96.37 dBc/Hz, and -107.37 dBc/Hz at 100 kHz, 1 MHz, and 10 MHz respectively. The power consumption is 28 mW with 1.2-V supply voltage.**

Keywords-CMOS, Meta-material, Voltage Controlled Oscillator (VCO)

I. INTRODUCTION

Meta-material is artificial structure having the property that does not exist in nature, it enables to realize radio wave characteristics which are impossible in practical like negative permittivity or negative permeability [1]. If meta-material is applied to analog circuit design, the properties not exist in the conventional circuits could be possible.

In this paper, we apply meta-structure to VCO (Voltage-Controlled Oscillator) periodically to improve the phase noise characteristic, and a novel CMOS based META-VCO (meta-material VCO) is proposed.

II. META-STRUCTURE AND VCO DESIGN

A. *Meta-structure design*

Meta-structure is implemented by arranging SRR (Split Ring Resonator) to obtain negative permeability [1]. The proposed meta-structure is shown in Fig. 1.

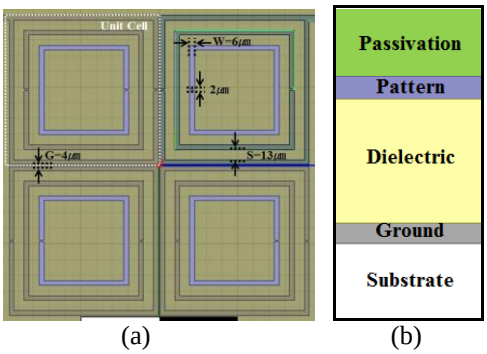


Fig. 1. Meta structure (a)top view (b)cross-section

The inductance is designed by the length of the pattern and the capacitance is designed by the gap between pattern and ground or pattern and pattern. Therefore, the desired frequency characteristic of the LC resonance could be obtained by adjusting the width and length of the pattern, the dielectric thickness, and the distance between the pattern and the pattern. Using these properties, we replaced LC resonator with the proposed meta-structure. We used HFSS CAD tool to analyze the property of the meta-structure. By the thickness of the layers, the relative permittivity, the relative permeability, conductivity, and so on of the process, we could organize materials composing meta-structure. In Fig. 1.(b), the thickness of the passivation is 11μm, the pattern is 1.3μm, dielectric is 7.1μm, ground is 1.1μm and substrate is 780μm.

B. *VCO design*

The schematic and size of the VCO applying the meta-structure is shown in Fig. 2. The architecture of the proposed META-VCO is composed of LC resonator of the meta-structure, NMOS cross-coupled differential structure to generate negative resistance, and two varactors to control resonance frequency. The oscillation frequency becomes low because of the capacitance of the varactor. MN3 and MN4 are output buffer, and VDDA and VDDB are separated to prevent the noise influence from the noise of the output buffer. R_{ISOL} is very small resistor with the value of 4Ω, and helps to reduce the noise of the power supply in measurement environment.

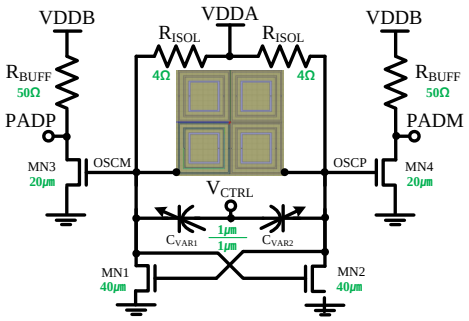


Fig. 1. Schematic of the META-VCO

III. CIRCUIT IMPLEMENTATION AND MEASUREMENT RESULTS

The proposed META-VCO was implemented using 65nm CMOS process and the area is $0.51\times0.49mm^2$ as shown in Fig. 3. In the measurement, on-wafer probing was carried out using the probe station, N9010A spectrum analyzer, and dual power supply. The Infinity probe could measure the output of the META-VCO, while GSSG monitors ground-signal-signal-ground. VDDA and VDDB are 1.2-V and it was confirmed that the output frequency was varying according to V_{CTRL}. Fig. 4

show the output frequency and the output power when V_{CTRL} was 0-V and 1.2-V. We compensated the losses of the cable and probe in the measurement environment, and the compensated output powers were -19.12 dBm and -22.12 dBm at 8.45 GHz and 8.77 GHz respectively. The measured phase noises were -67.8 dBc/Hz, -96.37 dBc/Hz, and -107.37 dBc/Hz at 100 kHz, 1 MHz, and 10 MHz respectively as shown in Fig. 5. The power consumption of the META-VCO was 28 mW.

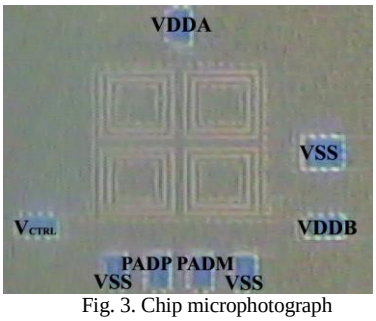
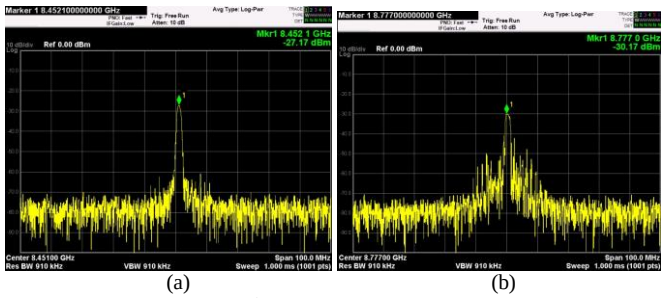


Fig. 3. Chip microphotograph


(a) (b)
Fig. 4. Measured output frequency at (a)V_{CTRL}=0-V (b) V_{CTRL}=1.2-V

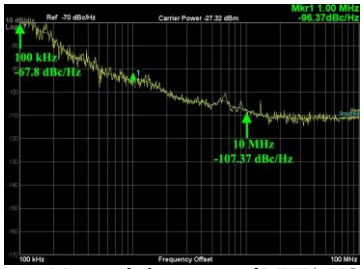


Fig. 1. Measured phase noise of META-VCO

The proposed META-VCO was compared to other works to verify its performance by using measured values. Following FOM equation was used for the evaluation and is defined in Eq. (1) [2]:

$$FOM_T = L\{\Delta f\} - 20\log\left(\frac{f_0}{\Delta f}\right) + 10\log\left(\frac{P_{DC}}{1mW}\right) \qquad (1)$$

Here, $L\{\Delta f\}$ is the phase noise, Δf is the offset frequency, f_0 is the oscillation frequency, and P_{DC} is the power consumption of the VCO. Smaller FOM means the better performance of the VCO and the FOM of the designed META-VCO is about -140.76 dBc/Hz. Table I summarizes the performance comparison between the proposed work and recently reported works, and we confirmed the good phase noise. So, the proposed META-VCO using meta-structure has an advantage in phase noise performance.

TABLE I. PERFORNANCE SUMMARY AND COMPARISONS

	*[3]EUROCON 2013	*[4]TCSI 2013	This work
Process	**90 nm CMOS**	**130 nm CMOS**	**65 nm CMOS**
Operating frequency [GHz]	**0.6-11.8**	**5.92-13.52**	**8.45-8.77**
Phase noise [dBc/Hz]	**-73.9@1 MHz**	**-69.3@1 MHz**	**-67.8@100 kHz -96.37@1 MHz -107.37@10 MHz**
Output power [dBm]	**N/A**	**N/A**	**-19.12**
P_{DC} [mW]	**22**	**31.69**	**28**
FOM [dBc/Hz]	**-136.04**	**-133.38**	**-140.76**
Supply [V]	**1.2**	**1.2**	**1.2**

*Simulation results

IV. CONCLUSIONS

A low phase noise VCO using 65nm CMOS process with meta-structure was designed in this work. The meta-structure is analyzed by HFSS and the META-VCO is simulated by CADENCE Spectre RF.

In measurement results, META-VCO operated 8.45~8.77 GHz according to V_{CTRL}, and the output power was -19.12 dBm. The phase noises were -67.8 dBc/Hz, -96.37 dBc/Hz, and -107.37 dBc/Hz at 100 kHz, 1 MHz, and 10 MHz respectively. The power consumption was 28 mW with 1.2-V supply voltage.

In this work, we shows the feasiblity that meta-structure could be applied to CMOS process by the chip implementation and measurement. VCO is the one of the most important block of the frequency synthesizer [3-4], so the proposed META-VCO could be applied to digital system core clock generator and communication system which needs several GHz frequencies.

ACKNOWLEDGMENT

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