A study of META-Voltage Controlled Oscillator and Prescaler using 65nm CMOS Process

META-VCO and Prescaler using 65nm CMOS Precess

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***Abstract*— The VCO (Voltage Controlled Oscillator) and the high speed prescaler are designed using 65nm CMOS technology with the frequency of 28.5GHz 5G mobile communication system. The simulation result show that the VCO has 28.4~28.8GHz tuning range and the prescaler divides the VCO output. The phase noise of the VCO is -173.75dBc/Hz at 1MHz and -181.43dBc/Hz at 10MHz offset frequency.**

VCO; Prescaler; 5G; phase noise; (key words)

I. INTRODUCTION

Due to the development of the mobile communication device, the wireless data usage is increasing. The data usage is beyond the range that can be accommodated in the existing 4G networks (LTE / WiBro) after 2020. So, 5G-network are being developed as next-generation mobile communications. 5G network transmits the data fast by using the ultra-high frequency band of 20GHz ~ 40GHz. The PLL is used to generate ultra-high frequency stably, the block diagram is shown in Figure 1. The voltage controlled oscillator to generate high frequency exists in the PLL. The frequency divider block is used to lower ultra-high-frequency to low-frequency. In this paper, the voltage-controlled oscillator and prescaler were designed using 65nm CMOS process.

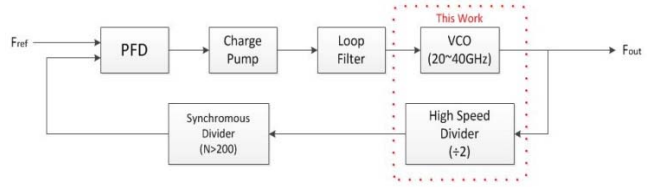

Figure1. 29 GHz PLL for the wireless communication system.

II. EASE OF USE

A. Meta-structure for the proposed VCO

Meta-material is used to have special electrical properties that can not be found in nature. In this paper, we use the SRR structure by controlling the variables of the SRR structure to obtain the LC resonance characteristics. Figure 2 shows the proposed meta-structure resonator array.

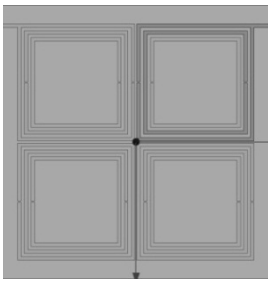

Figure 2. LC resonator structure of the SRR array (top view)

B. META-VCO

Figure 3 show the META-VCO circuit using the meta-material designed using HFSS. The META-VCO is composed of meta-material for the inductor role, NMOS cross coupled pair having negative resistance, and two varactors (C_{VAR1} and C_{VAR2}). It was designed to control the oscillation frequency by adjusting V_{CTRL}. Because meta-material has the parasitic capacitance, the parasitic capacitance of META-VCO is larger than the conventional LC-VCO. So we have designed the meta-material having high operating frequency to obtain operating frequency of 28.5GHz. R_{ISOL} is very small resistance less than 15Ω. It prevents short circuit of the OSCP and OSCM node to the VDD.

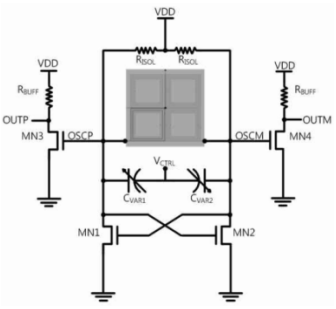

Figure 3. META-VCO circuit

C. Prescaler

The VCO frequency (F_{VCO}) is divided to several tens of MHz in PLL.

The CML-divider consists of two latches. The sample pair in the master latch and the hold pair in the slave latch are operated when CLK is 'high'. The hold pair in the master

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latch and the sample pair in the slave latch are operated when CLK is 'low'. Since the output is connected to the input as negative feedback, CLK frequency should be in the operating frequency range of the frequency divider, so CML-divider outputs the frequency divided signal from the CLK.

In this paper, we proposed the structure as shown in Figure 4, which replaces the resistance error in the layout of PMOS. The proposed architecture is composed of sample pair and hold pair. The sample pair is connected PMOS but hold pair is not connected. The sample pair was designed with twice W / L ratio of the hold-pair to send larger current to the sample pair.

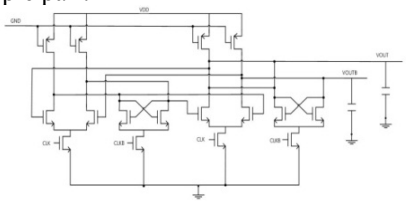


Figure 4. The proposed structure of CML divider

III. IMPLEMENTATION

Figure 5 shows the resonance frequency characteristic. S_{11} is -26.4dB and S_{21} is -12.1dB. Figure 6 shows The META-VCO simulation results. The META-VCO has the operating range of 28.4 ~ 28.8GHz by controlling V_{CTRL}. The phase noise at 1MHz offset frequency is -173.75dBc / Hz, 10MHz offset frequency is -181.43dBc / Hz.

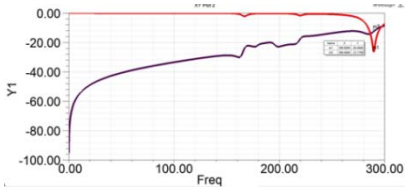
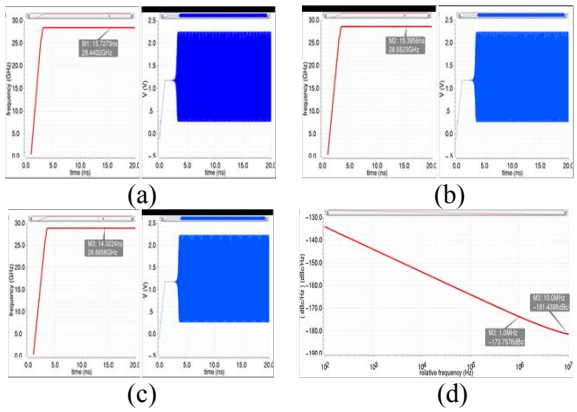


Figure 5. HFSS resonant characteristics graph of the proposed META structure



(a) (b) (c) (d)

Figure 6. (a) V_{CTRL} = 0V (b) V_{CTRL} = 0.6V (c) V_{CTRL} = 1.2V (d) Phase noise

The output of the VCO is 28.8GHz when V_{CTRL} = 1.2V. Figure 7 shows the waveform of the VCO and the frequency divider. Output waveform after passing the divider is shown in figure 6, and the frequency is about 14GHz. The final output waveform of the divider has the output swing of 440mV.

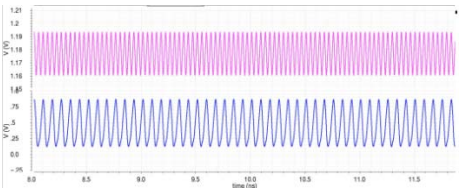


Figure 7. Simulation results prescaler

IV. CONCLUSIONS AND FUTURE RESEARCH DIRECTIONS

We designed the VCO using meta-structure based on the CMOS process in this study and the high-speed divider for dividing the frequencies using with CMOS technology. It was confirmed by the simulation for high-speed data transmission at high frequency. In this study META-VCO and CML are applicable for PLL which is operating at mm-wave frequency range.

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