A design of Dual-band Smart Tag

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***Abstract*— The dual-band smart tag is designed and is fabricated using a 0.18 ㎛ 1-Poly 4-Metal CMOS Process, and the area is 5mm × 5mm. The dual-band smart tag can recognize and demodulate the frequency bands of both UHF band (868 ~ 956 MHz) and HF band (13.56 MHz). The Digital block for verification is programmed in Arduino Uno board. Consequently, the dual-band smart tag communicates between the HF/UHF reader and the tag.**

Keywords—dual-band smart tag; RFID; NFC;

I. INTRODUCTION

RFID(Radio-Frequency Identification), the technology to recognize information in the radio-wave of near / far distance, uses various frequency bands. HFID(High-Frequency Identification) named NFC(Near Field Communication) uses the frequency band of 13.56 MHz, and it has been applied to the access control systems, electronic cash, transportation card, and smart card. UHFID(Ultra High-Frequency Identification) uses the frequency band of between 868 MHz and 956 MHz, and it has been applied to the distribution, logistics, SCM(Supply chain management), and automatic toll collection. The current distribution and logistics system uses HF and UHF systems concurrently. It is very ineffective, because current system uses different tags in the same radio system. In this paper, we have designed the Smart Tag for the transmission of the two bands and the verification of the Digital block has been completed by using the Arduino Uno board.

II. THE DESIGN OF DUAL-BAND SMART TAG

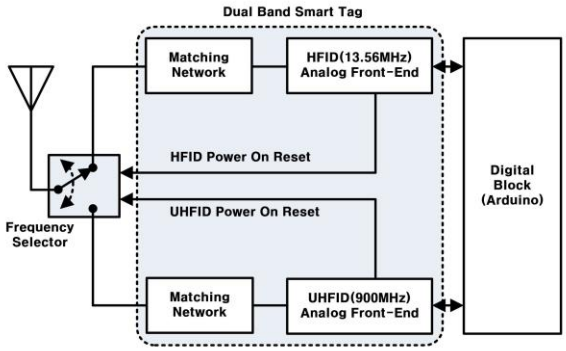

Figure 1. Block diagram of the proposed dual-band smart tag

Figure 1. shows the block diagram of the proposed dual-band smart tag. It consists of the analog front-end and the frequency selector. The analog front-end transmits and receives individual data of both HF and UHF bands. The frequency selector distinguishes between HF and UHF signals, each the analog front-end is operated according to the output voltage of the frequency selector.

A. The analog front-end

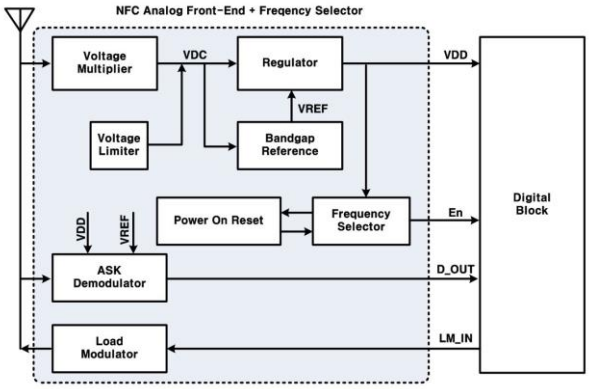

Figure 2. Block diagram of the proposed analog front-end

Figure 2. shows the block diagram of the proposed analog front-end. The analog front-end consists of the power supply part, the ASK demodulator and the load modulator. Using the signal received from the reader, the power supply part generates the energy for supplying the current to the internal circuit. The voltage multiplier generates the large DC voltage due to the multi-stage structure. The voltage limiter is required because large DC voltage may cause damage to the internal circuitry. The bandgap reference and the regulator generate stable DC voltage to supply the VDD for other circuits. The ASK demodulator generates digital data and transmits them to the digital block, and the load modulator sends the reader response signal from the digital block. The power supply part composed of the DC rectifier to convert the AC signal to DC signal, the voltage multiplier, the bandgap reference, the regulator, the voltage limiter to prevent the damage of internal circuit, and the power-on reset circuit to reset digital block after data transmission.

B. The frequency selector

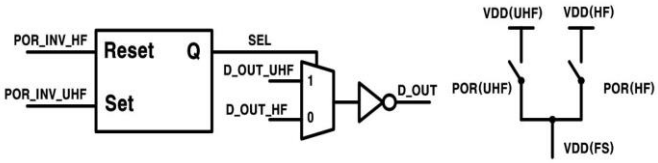

Figure 3. The proposed frequency selector circuit

Figure 3. shows the proposed frequency selector circuit. Two signals from the dual-band antenna enter the frequency selector. It distinguishes between HF and UHF signals. If the frequency selector decides the signal as the HF signal, the HF analog front-end is turned on. If the frequency selector decides

the signal as the UHF signal, the UHF analog front-end is turned on.

III. MEASUREMENT RESULT

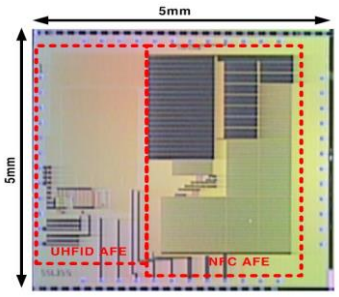

Figure 4. Photograph of the dual-band smart-tag chip

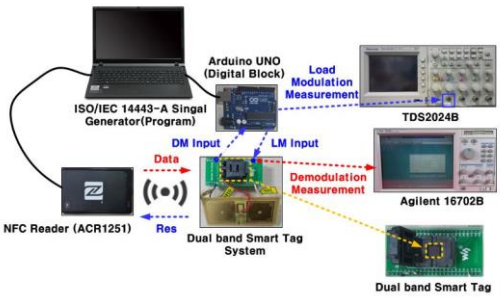

Figure 5. Measurement Environment

Figure 4. shows the photograph of the dual-band smart tag chip. We used a 0.18μm 1-Poly 4-Metal CMOS Process, and the area is 5mm×5mm. Figure 5. shows the measurement environment to measure the Test board. The NFC reader (ACR1251) generates the input signal of the ASK 100% satisfied the ISO/IEC-14443A standard. After receiving the input signal, we measured the test board output. The amplitude changes according to the response signal and the demodulated signal is measured using the TDS2024B (Oscilloscope).

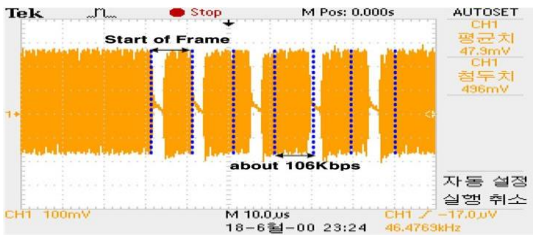

Figure 6. Measurement of the reader signal

Figure 6. shows the result of measurement of the ALL_REQ signal requesting the response to the digital block. Figure 7. shows the demodulation signal after receiving the ALL_REQ. The demodulation has been completed, the digital signal enter into the input of the Arduino Uno, and the program distinguishes both High("1") and Low("0"), and sends the response signal of 847KHz bit rate with Manchester coding.

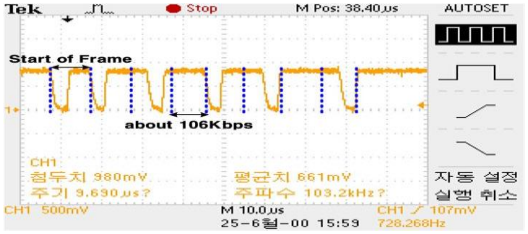

Figure 7. Measurement of the demodulation signal

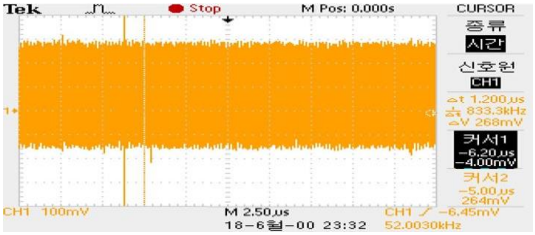

Figure 8. The signal prior to sending the response signal

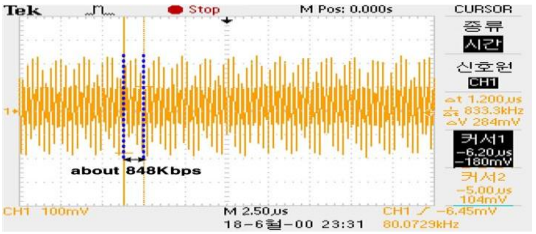

Figure 9. The signal after sending the response signal

Figure 8. shows the signal between the reader and the antenna prior to sending the response signal. Figure 9. shows the signal between the read and the antenna after sending the response signal. The amplitude change of signal can be seen from the measurement when the reader and the tag communicate.

IV. CONCLUSION

We have designed the dual-band smart tag. According to the induced signal, the test board produces the demodulated signals. We have integrated the Analog Front-End of UHF band and HF band in a single chip. The dual-band smart tag will replace the previous two tags and would be used widely in distribution and logistics systems.

ACKNOWLEDGMENT

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