# A design of NFC Analog Front-End with the Frequency Selector

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*Abstract*— **We have designed the NFC analog front-end including the frequency selector using 0.18μm CMOS Process. The NFC analog front-end satisfied the ISO/IEC-14443A/B. It consists of the power supply block and the data transmitter block. The power supply block has the DC rectifier, voltage multiplier, bandgap reference, and regulator. The data transmitter block has the demodulator and the load modulator. The frequency selector distinguishes NFC signal which satisfies the ISO/IEC-14443A standard and the wireless power transfer signal which satisfies Rezence standard. If the frequency selector receives the frequency signal of 6.78MHz, output becomes 1V. If the frequency selector receives the frequency signal of 13.56MHz, output becomes 0V and the data transmitter block of NFC analog front-end is turned on.**

***Keywords; NFC , Rezence, wireless power trasnfer tag.***

## I. INTRODUCTION

NFC (Near Field Communication) uses 13.56MHz of high frequency band and communicates the distance of 10cm between reader and tag. It also satisfied the ISO/IEC-18092 and ISO/IEC-14443A/B standards. It has been applied to the Smart Card like a transportation card, access control and electronic cash. WPT (Wireless Power Transfer) for wireless charging has the two methods in wireless charging market. One is inductive method, and the other is resonant method. Recently inductive method takes the lead in wireless charging market. Inductive method has the Qi Standard of WPC (Wireless Power consortium) and PMA (Power Matters Alliance) standard. A4WP (Alliance for Wireless Power) founded in 2012 uses resonant method and named the standard as Rezence. Presently A4WP and PMA incorporated Air fuel Alliance to lead the wireless charging market in the near future. The proposed NFC analog front-end with the frequency selector satisfied the standard of ISO/IEC-14443A and the Rezence of A4WP. The proposed circuit shares the supply block of NFC analog front-end. The supply block is operated according to the input frequency signal. If the input frequency signal is 13.56MHz, supply block output is connected to demodulator for NFC data transmit to send the demodulated data. If the input frequency signal is 6.78MHz, supply block output is connected to the wireless battery charging block.

TABLE I. DESIGN SPECIFICATION

| | ***NFC*** | ***Wireless Charging*** |
|---|---|---|
| ***Standard*** | ISO/IEC-14443A | Rezence |
| ***Frequency band*** | 13.56MHz | 6.78MHz |
| ***Operation Mode*** | Passive | - |
| ***Supply Voltage*** | 1V | |

## II. THE NFC ANALOG FRONT-END WITH THE FREQUENCY SELECTOR

### A. *The NFC analog front-end*

The block diagram of the proposed NFC analog front-end with the frequency selector is shown in Figure 1.

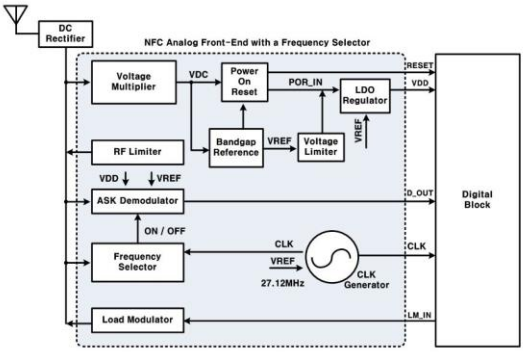


Figure 1. The block diagram of the proposed NFC analog front-end with the frequency selector

The NFC analog front-end consists of the power supply block and the data transmitter block. The power supply block supplies stable DC Voltage to the ASK demodulator, the clock generator and the digital block. For generating the stable DC voltage, the power supply block has the voltage multiplier, the bandgap reference and the regulator. At first, the voltage multiplier generates large DC voltage due to the multi-Stage structure. And the voltage limiter is required because large DC voltage may cause damage to the internal circuitry. The DC voltage generated by the voltage multiplier is unstable. So the bandgap reference and the regulator generate stable DC voltage to supply the VDD for other circuitry. The data transmitter block has the ASK demodulator and the load modulator. The ASK demodulator transmits data to the digital block. The power of the circuit is supplied from the power supply block. The load modulator responds data from the digital block. The clock generator supplies the constant clock to digital block for the synchronization of input signals.

### B. *The frequency selector*

The proposed NFC analog front-end has two functions. At first, it transmits data to the digital block for NFC communication. At second, it supplies DC voltage to the wireless battery charging block. So the NFC analog front-end has to distinguish two frequency bands and the frequency

selector performs this function. Figure 2. shows the proposed frequency selector circuit.

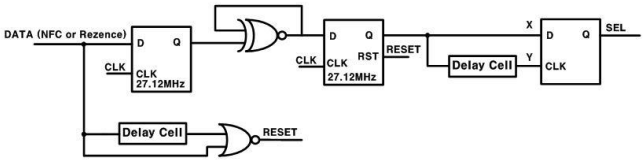


Figure 2. The proposed frequency selector circuit

The first Flip-Flop performs the synchronization between the internal clock (output of the clock generater) and the input signal. We used the internal clock of 27.12MHz. This frequency is 4 times of the Rezence standard frequency period and twice of the NFC standard frequency period. After the synchronization, the input signals are compared with the internal clock. If the frequency selector receives the frequency signal of 6.78MHz (wireless charging signal), output becomes 1V. If the frequency selector receives the frequency signal of 13.56MHz (NFC), output becomes 0V. Because the reader sends the ASK 100% signal including the 0V data, the output of the frequency selector data have to be 0V.

## III. SIMULATION RESULTS

### A. *The NFC analog front-end*

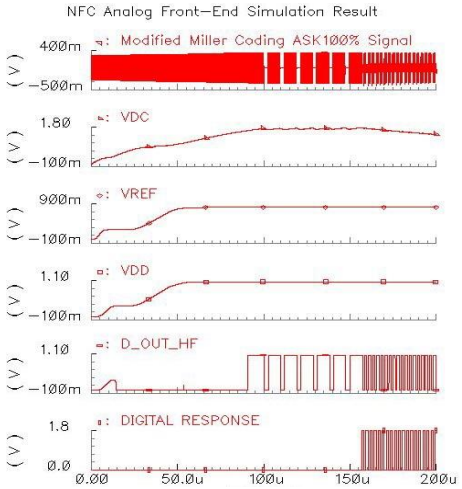


Figure 3. The NFC analog front-end simulation result

Figure 3. shows the simulation result of the NFC analog front-end consists of the power supply block and the data transmitter block. The ASK signal using modified Miller coding from the reader goes into the voltage multiplier. It makes the output voltage, VDC. The voltage limiter did not work because the voltage of the ASK signal which is entering is low at this simulation. The bandgap reference supplied the output voltage of the DC rectifier (VDC). The bandgap reference outputs the constant voltage (VREF). After the regulator receives VREF from the bandgap reference, VDD can be obtained through the error amplifier operation of the regulator. It is used as the supply voltage (VDD) of the NFC analog front-end. D_OUT_HF shows the operation of demodulation. The digital block received the data through the operation of demodulation and sends the response signal (DIGTAL RESPONSE).

The response signal based on Manchester coding has the carrier frequency of 847 KHz, the amplitude of the input signal changing at the rate of 847 KHz by receiving the response signal.

### B. *The frequency selector*

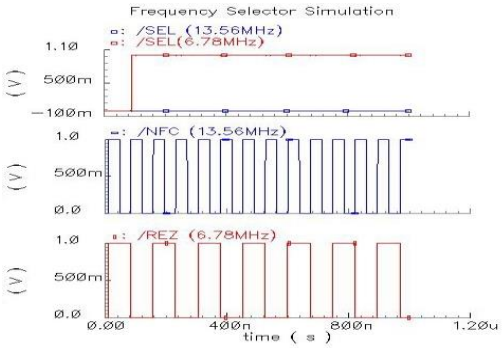


Figure 4. The frequency selector simulation result

Figure 4. shows the simulation result of the frequency selector. NFC signal has the frequency of 13.56MHz, REZ (Rezence standard signal) has the twice period of the NFC signal. Two signals are compared with the internal clock of 27.12MHz. If the input signal has the frequency of 6.78MHz, output voltage becomes 1V. If the input signal has the frequency of 13.56MHz, the output voltage becomes 0V. SEL is the output voltage of the frequency selector in this simulation

## IV. CONCLUSION

We have designed the NFC analog front-end including the frequency selector using 0.18μm CMOS Process. The frequency selector circuit has two functions. If the input signal operates at the frequency of NFC, the frequency selector output becomes 1V and the NFC analog front-end internal circuit is turned off. If the input signal operates at the frequency of the wireless charging signal (Rezence), the frequency selector output becomes 0V and NFC analog front-end block is turned on.


## ACKNOWLEDGMENT

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