A study of the referenceless CDR based on PLL

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Abstract— Clock data recovery (CDR) circuit is an essential component for serial data communication. S/PDIF which is one of data coding is used. The CDR based on PLL recovers clock and data of 2.8224 ~ 24.576MHz and was designed with the frequency detector (FD) to detect the frequency by using the preamble. The PLL, frequency detector (FD) and the reset circuits were used to design the refernceless CDR based on PLL. 65nm CMOS process is used in this study.

Keywords CMOS, CDR , SPDIF , PLL , Frequency Detector, CDR based-on PLL

I. INTRODUCTION

Clock data recovery (CDR) circuit is an essential component for serial data communication. The clock information is included in digital coded data. For this reason, CDR circuits are important to the clock and data restoration of digital coded data. Recovery circuit could be designed in several different ways. Most of CDR circuits are based on PLL. CDR based on PLL is classified as reference CDR and referenceless CDR. Referenceless CDR is better than reference CDR in cost. Because it does not use of crystal oscillator in receiver [1] [2].

This paper uses the S/PDIF signal which is one of data coding. SPDIF is the acronym of Sony / Philips Digital Interface Format, data protocol for transmitting digital audio signals. SPDIF digital data stream is encoded using the BMC (Bi-phase Mark Code). SPDIF signal has 192 frames in one block. One frame has two sub-frames. The preamble signal of 8bits exists in each the sub-frame. In addition, other S/PDIF features follow the standard IEC-60958 [3].

The proposed CDR could cover the full range of SPDIF. The frequency detector is designed to detect the sampling rate change in S/PDIF. Reset circuit is designed and described from the following chapters.

II. ARCHITECTURE

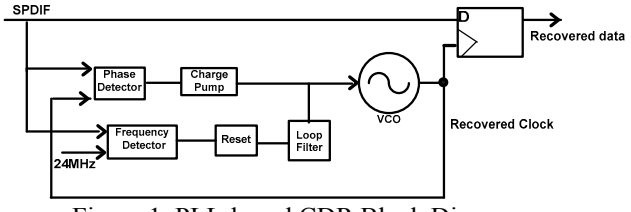

Figure 1. PLL-based CDR Block Diagram

Figure 1 is the block diagram of CDR based on PLL using reset signal. The operation of CDR is described in detail. S/PDIF is the input signal. The phase locked loop (PLL) block recovers clock in SPDIF signal. PLL block is locked to the recovered clock. When the sampling rate changes in S/PDIF, frequency detector (FD) are designed to detect the frequency change. When the change in frequency is detected, FD generates 3 bit signals.3bit signals generate the RESET signal. If the RESET again signal is detected, PLL block find the target frequency.

A. Frequency Detector design

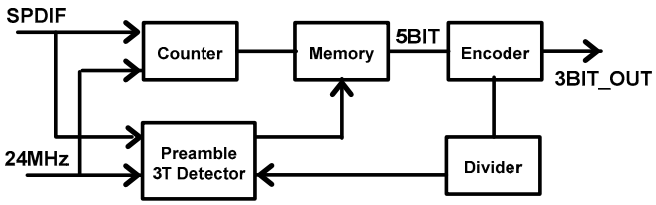

Figure 2. Frequency Detector Block Diagram

Figure 2 is the block diagram of the frequency detector. Frequency detector sample is SPDIF signal according to 24MHz clock. If frequency detector detects the preamble, stores the count value in the memory block. The frequency detector can detect the frequency using the preamble. After the detection of the frequency from preamble, frequency detector outputs 3bit signals corresponding to the detected frequency.

B. The PLL-based CDR

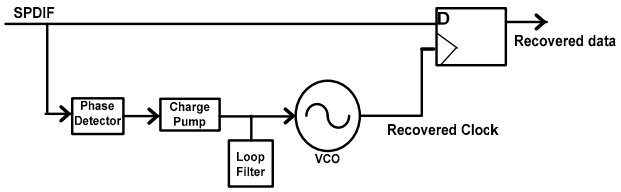

Figure 3. The CDR based on PLL Block Diagram

Figure 3 is the block diagram of the PLL-based CDR. The Voltage Controlled Oscillator (VCO) of the CDR based on PLL is composed of the ring oscillator 5 stage inverter with feedback loop. The oscillation frequency of VCO is determined by the amount of current passing through the inverters. CDR should use support the full range of SPDIF. The input signal of CDR circuit is random data. Phase frequency detector (PFD) of the conventional PLL could not be used, because the output value of PFD follows CDR follows random data, so CDR loses the lock condition. Therefore, the hogge Phase Detector (PD) is used [4]. The

pumping current of charge pump circuit is 60uA. D flip flop is master and slave type. The third order loop filter used.

C. *Reset circuit*

Figure 5. The Multivibrator Reset Block Diagram

Fig 5 is the block diagram of multivibrator reset circuit .When sampling rate changes, 3 bit signals show the transition. The RESET signal duration is generated by monostable multivibrator circuit.

III. MEASUREMENT AND CONCLUSION

The simulation results are as follows

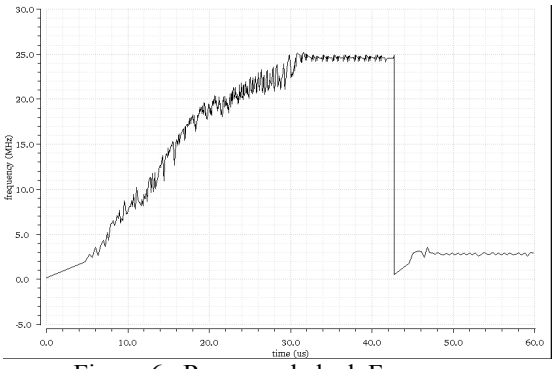

Figure 6. Recovered clock Frequency

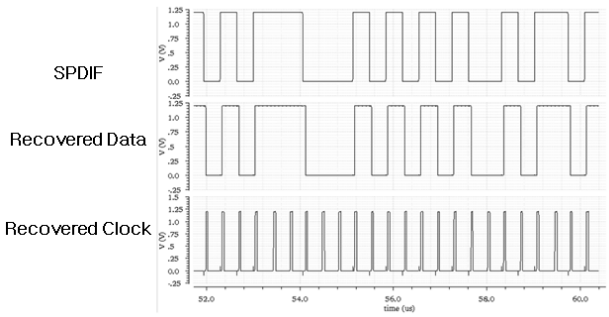

Figure 7. SPDIF/ Recovered clock / Recovered data Graph

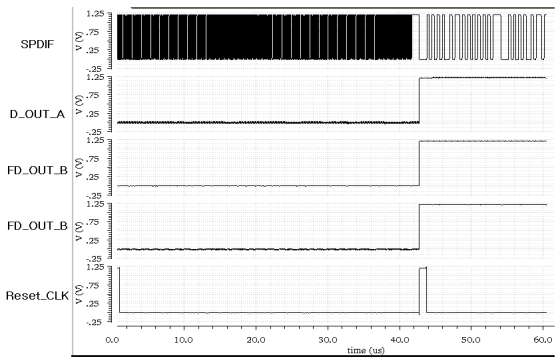

Figure 8. SPDIF / FD OUTPUT_A,B,C / Reset_CLK

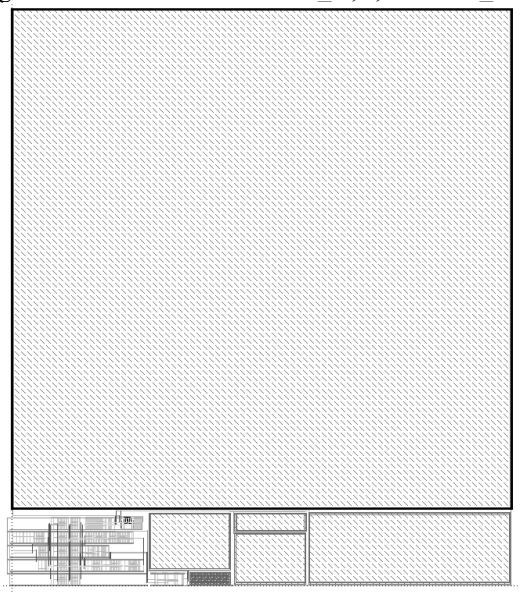

Figure 9. PLL-based CDR Block Layout

Figure 6 shows the post simulation result of the recovered frequency of the SPDIF using the CDR. This shows the change in frequency from 24.576MHz to 2.8224MHz.

Figure 7 shows the transient simulation result. Recovered clock, recovered data and S/PDIF signals are shown in plot.

Figure 8 is shows FD OUTPUT_A, B, C and RESET_CLK signal. When the sampling rate changes in S/PDIF, PD operates. 3 bit signals of FD simulation are result. RESET_CLK is generated after 3 bits has passed Multivibrator Reset circuit.

Clock and data is recovered according to S/PDIF change. The CDR circuit has been designed in a 65nm CMOS technology. The layout is shown in Figure 9. CDR layout size occupies the area of 502 um x 581um.

IV. ACKNOWLEDGMENT

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V. REFERENCES

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