A design of Sigma Delta modulator for Frequency Synthesizer

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Abstract – This paper presents A 16bit 3rd order single loop Sigma Delta Modulator for Frequency Synthesizer with comparison Frequency 140MHz.. Sigma Delta Modulator suppress fractional spurious tones while reducing in band phase noise and control dividing ratio between N divider and N+1 divider. Using MATLAB simulation ensures that the modulator operates under the stable status and calculates Optimized Coefficient of Transfer Function. Sigma Delta Modulator has been implemented 0.35 ㎛ CMOS 1-poly and 4-metal process with 3.3V supplies voltage. The functional operation of the modulator has been verified through structural bit-level simulations as well as experimental result on actual implementation

Keywords: Sigma Delta Modulator, Noise Shaping, fractional spur, phase noise, stability, optimized coefficient

1 Introduction

Frequency synthesizer is used widely in integrated circuit for present radio communication. Frequency synthesizer based on PLL is essential to generate correct and desired frequency. Frequency synthesizer[1][2] takes out other frequency ingredient using for fixed standard frequency and so on. Fractional-N Frequency synthesizers have shown good performance in the view points of fast switching time, fine frequency resolution, and negligible spurs. frequency synthesis using Fractional–N PLL based on Sigma Delta Modulator offers wide bandwidth with narrow channel spacing and alleviates PLL design constraints for phase noise and reference spur. However, the synthesizer phase noise performance is significantly affected by high-frequency out of band noise which is difficult to suppress with the finite number of PLL loop filter poles. Sigma Delta Modulator is currently a very popular technique for its low-complexity of analog circuitry and robustness. Sigma Delta Modulation method is a standard fractional techniques alternate the divide value between N and (N+1) in some duty cycle that produces the desired fractional value between N and (N+1),The division value is integer at any time, but the average value has fractional value. [2][3][4]

In this paper, The architecture and design of Sigma Delta Modulator is described in Section 2. Simulation and verification is described in section.3, chip implementation and test result are covered in section. 4. Finally, conclusions are summarized in section. 5.

2 Sigma Delta modulator Architecture

2.1 Architecture of Frequency Synthesizer

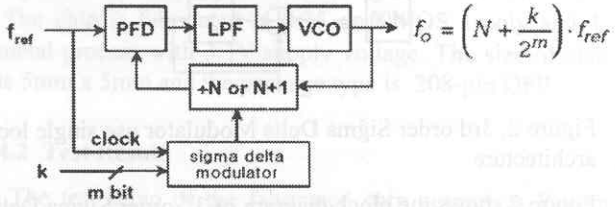

Figure 1. Sigma Delta Modulator in Fractional-N Frequency Synthesizer

Figure1shows the block diagram of Frequency Synthesizer. Fractional-N Frequency Synthesizer is composed of a voltage-controlled oscillator (VCO), a phase frequency detector(PFD), a frequency divider and eventually a loop filter and Sigma Delta Modulator. Sigma Delta Modulator controls dividing ratio of N/(N+1) divider. The reference frequency for comparison is known as F_{REF}.

The ratio that (N+1) dividing happens is known as N_{FRC} .The relationship between above parameters are follows

$$F_{REF} = \frac{F_{VCO}}{N + N_{FRC}} \Rightarrow F_{VCO} = (N + N_{FRC}) \bullet F_{REF}$$

(N is integer, $0 \le N_{FRC} \langle 1$)

So the synthesized frequency is fractional times of reference frequency controlling the dividing ratio of frequency synthesizer properly by Sigma Delta Modulator. The dividing ratio lies between N and (N+1).

2.2 The design of 3rd Sigma delta Modulator

First order Sigma Delta Modulator is simple but noise shaping capability is small. More than second order modulator is needed to remove Noise effectively [5][6].

Sigma Delta Modulator design is changed according to order, number of stage and quantization bit level. There are single loop structure and cascade structure according to number of stage. If we use high order Sigma Delta Modulator using single loop architecture, circuit design is simple. But Sigma Delta Modulator could be unstable. Modulator should be stable always, so we should control the gain of integrator. In this paper, we propose 3rd order Sigma Delta Modulator which suppress noise power below -100dB in loop Bandwidth.

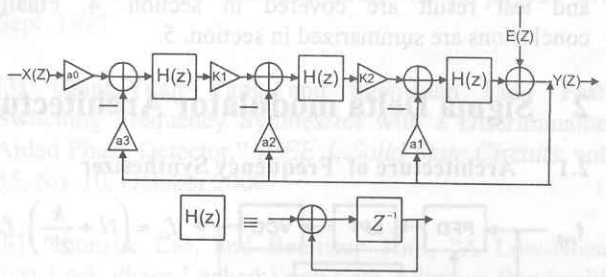

Figure 2. 3rd order Sigma Delta Modulator use single loop architecture

Figure 2 shows the block diagram of 3rd order Sigma Delta Modulator using single loop architecture. Equation (1) is Noise Transfer Function of Figure 2.

$$H(z)_{NTF}=\frac{(z-1)^3}{z^3+(a1-3)z^2+(a2-2a1+3)z+a3-a2+a1-1} \quad (1)$$

The key of Fractional-N frequency synthesis based on Sigma Delta Modulators design is obtaining optimized coefficient. And, logic verification is also important . Modulator loop must contain at least one delay block in design. If delay block is not include in modulator, the modulator would be an inconsistent and unrealizable system. Delay block is included in H(z) block in this design. Butterworth filter of desired frequency characteristic to design and verify frequency characteristics should be designed first. The frequency characteristics are verified MATLAB simulation . We calculate coefficient using the transfer function of Sigma Delta Modulator that have the same characteristic of Butterworth filter. We calculate coefficient that satisfy following characteristics

F_{REF}	Bandwidth	Cutoff Freq.	Highpass Characteristic	Stable state
140MHz	20MHz	800MHz		

Table 1.. Butterworth Characteristic

It is Cutoff freq = 800MHz and Highpass Characteristic's Butterworth filter which has the cutoff frequency of 800MHz and Highpass characteristic is shown in equation (2)

$$H(S)=\frac{S^3}{S^3+0.4252\,S^2+0.0904\,S+0.0096} \quad (2)$$

Bilinear Transform changes s-domain to z-domain and The characteristic of bilinear transformed digital filter is the same as Butterworth filter.

$$H(z)=\frac{(z-1)^3}{z^3-2.168z^2+1.648z-0.430} \quad (3)$$

NTF out of gain = 1.5251

To make calculation conveniently, we assume a0 and a3 are the same. Coefficients are shown in Table 2.

a0	a1	a 2	a 3	K1	K2
0.050	0.832	0.313	0.050	0.313	0.050

Table 2. Optimized coefficient

By changing to K1 = 2^{-1} and K2 = 2^{-4} which could be easily implemented by digital logic like shift operation. To make circuit simpler, we set a0 by 1 and then rescales coefficient. If we set a3 as 65536, a1=34078 and a2=25641 by coefficient rescaling according to the proportional relationship.

a0	a1	a 2	a 3	K1	K2
1	34078	25641	65536	0.5	0.0625

Table 3. Rescaling Optimized Coefficients

Implementing Sigma Delta Modulator using calculated optimized coefficient needs adder and accumulator. Confirming the noise shaping level of modulator needs sample number more than 65536.

3 Simulation and Verification

3.1 MATLAB Simulation

The proposed Sigma Delta Modulator is verified by behavioral simulation using Simul-LINK MATLAB [7]. From MATLAB simulation, Sigma Delta Modulator pushes the quantization noise to out of band. Using the simulation result, the gain of integrator which ensure stable operation is determined.

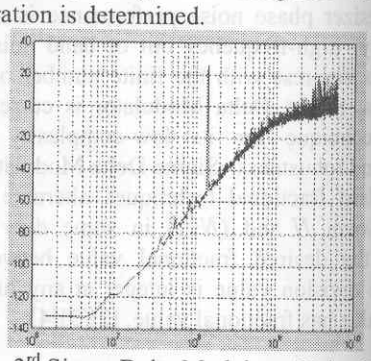

Figure 3. 3rd Sigma Delta Modulator Noise Spectrum

Figure 3. shows the noise spectrum simulation result . From the noise spectrum, it is easy to conclude that this modulator is stable. We can know that noise power becomes - 50 dB lower than 140MHz. The Peak of 140MHz in simulation happens because input frequency is the same as the reference frequency simulation. This problem happens only in simulation. So actual chip does not show the peak of 140MHz.

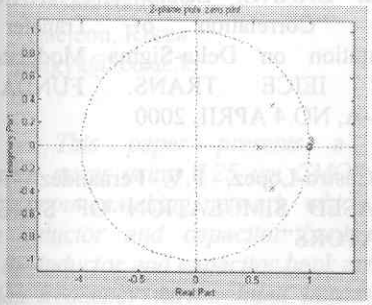

Figure 4. 3rd Sigma Delta Modulator Pole Zero location

Figure 4 shows the MATLAB behavioral model simulation result. NTF poles located in the unit circle of z-plane. MATLAB Simulation confirms the correctness of the proposed architecture.

3.2 Front-End Design and Verification

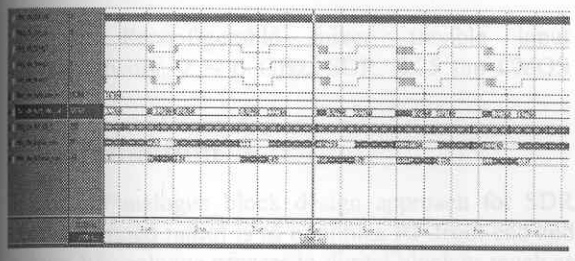

Figure 5. Modelsim Simulation

Figure 5 shows its MODELSIM behavioral model simulation result[9]. The 1bit quantizer output of Sigma Delta Modulator is 1 or – 1. It selects divider (N+1) when the quantizer output is 1 and select divider N when the quantizer output is -1. If input is 16bit value, output has 32768 and - 32768. If input value is 16384, output comes out 32768 150 times and -32768 50 times. The mean value is 16384. Bit stream (1 or - 1) that come out from output select N divider or (N+1) divider. The average value lies between N and (N+1), so the fractional dividing is obtained. We can see that average value is the same with input during enough fixed cycles.

4 Chip Implementation and Test Result

4.1 Chip layout

The Sigma Delta Modulator described in section 3.2 is designed by VHDL. And SYNOPSYS tool, Sigma Delta Modulator was synthesized. Gate Count is 9100 and core chip area is 1.5mm x 1.5mm. PnR is carried out by ASTRO using synthesized netlist. Figure 6 shows the chip layout after PnR is completed.

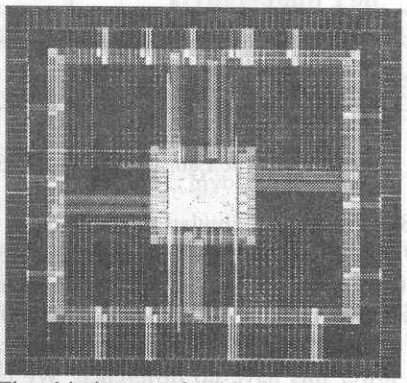

Figure 6. The chip layout of 16bit sigma delta modulator

The chip is fabricated in 0.35 μm CMOS 1-poly and 4-metal process with 3.3V supply voltage. The size of chip is 5mm x 5mm and the package type is 208-pin QFP.

4.2 Test Result

The test setup of the fabricated chip comprises Pattern Generator for input data, function generator for clock, oscilloscope, Logic Analyzer and DC power supply. Figure 7 Shows the block diagram of chip test environment.

In chip test, 16bit various kinds input is Need and input is generated by Pattern Generator.

After testing by oscilloscope, Logic Analyzer is used to confirm measurement value. The chip operation is verified by comparing the result of logic analyzer and the simulation result of MODELSIM.

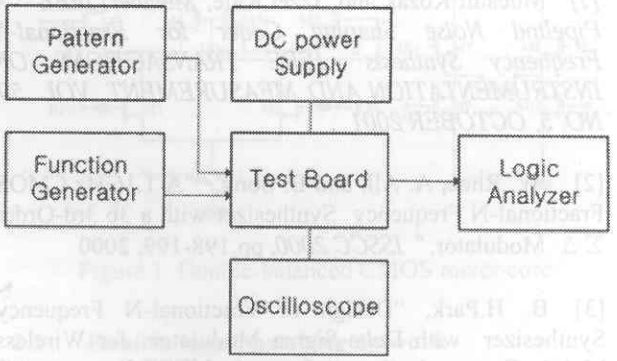

Figure 7 . The block diagram of chip test environment

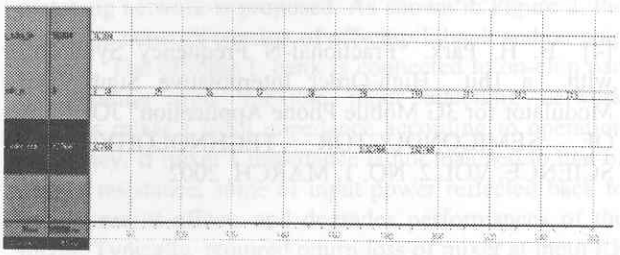

Figure 8. MODELSIM Functional Simulation

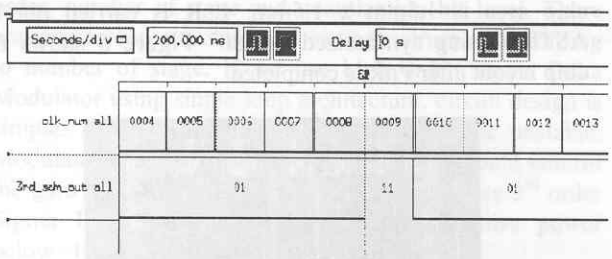

Figure 9. The Fabricated Chip TEST

Figure 8 is functional simulation result using VHDL and figure 9 is the test result of fabrication chip. The same input is used in test and simulation. When input is 16384, output has two value of 32768 (01000000000000000)and - 32768 (11000000000000000). MSB 2-bits are displayed, because lower bits have no difference. We could know that the test result and the simulation result are equal.

5 Conclusions

3rd single loop Sigma Delta Modulator for Frequency Synthesizer are designed using 0.35㎛ CMOS technology. MATLAB simulation confirms the correctness of the proposed architecture. The dividing ration of modulator is confirmed by MODELSIM simulation. The fabricated Chip shows the same result with the simulation result. Test with analog PLL will be performed and frequency synthesizer could be implemented using the proposed Sigma Delta Modulator.

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