An Adaptive Frequency Calibration Technique for Fast Locking Wide-Band Frequency Synthesizers

Tae-Won Ahn
Dept. of Electronics
Dongyang Technical College
Seoul, Korea
twahn@dongyang.ac.kr

Chan-Geun Yoon
Dept. of Infor. & Comm.
Dongyang Technical College
Seoul, Korea
cgyoon@dongyang.ac.kr

Yong Moon
School of Electronic Engineering
Soongsil University
Seoul, Korea
moony@ssu.ac.kr

***Abstract*— A fast response adaptive frequency calibration (AFC) technique for wide-band frequency synthesizers is presented. In order to operate in a wide-band frequency range, digitally controlled switched-capacitors bank LC VCO is used and a wide-range digital logic quadricorrelator (WDLQ) is proposed for frequency detector. The specified VCO tuning range is as wide as 1 GHz (50 %) from 1.5 to 2.5 GHz and the VCO gain is 20 MHz/V. The CADENCE Spectre simulation results show that the proposed design can achieve a fast adaptive frequency calibration in less than 25 μs with 10 MHz reference clock, which is shortened by half in comparison with the previous works which used counters for frequency detector.**

I. INTRODUCTION

In modern high-speed wireless communication systems, many RF transceivers need a fast-locking wide-band frequency synthesizer to provide various local oscillation signals for both transmitter and receiver [1]. The wide-band voltage-controlled oscillator (VCO) is a major concern for wide tuning features which are in high demand by the multi-band multi-mode transceivers [2]. There are two methods to implement a frequency synthesizer with wide frequency range. One simple method is to increase the VCO gain, which raises the ratio of frequency to the tuning voltage. However, as the VCO gain increases, the phase noise performance can be deteriorated due to frequency modulation. In addition, to cover wide frequency band of 1 GHz with low power supply voltage of 1.8 V, the VCO gain should be over 500 MHz/V, and this value is too high for recent low phase noise applications. The other method utilizes the switched-capacitors bank LC VCO and the adaptive frequency calibration (AFC) to achieve reduced VCO gain aw well as wide frequency band [3].

The AFC technique is used for not only extending the frequency band of the VCO but also reducing the lock time of the phase-locked loop (PLL)-based frequency synthesizer, which requires both the wide-range frequency detection capability and the fast response time. Early approach to the detection of frequency was based on the comparison of the frequency of the reference clock and the VCO feedback clock using counters and state machine to determine which clock is faster.

In this paper, we present a wide-range digital logic quadricorrelator (WDLQ) for frequency detector to implement the AFC for wide-band frequency synthesizer. The WDLQ has been extended from a digital logic quadricorrelator (DLQ) whose operation is based on Teager's analog energy tracker [4]-[5]. We show that the WDLQ circuit has wide detection range of +100% of the reference clock rate, and fast response time. In our simulation, the specified VCO tuning range is as wide as 1 GHz (50 %) from 1.5 to 2.5 GHz, VCO gain is 20 MHz/V, and 6-bit digitally controlled switched-capacitors bank LC tank with 20 MHz frequency resolution is used. The CADENCE Spectre simulation results show that the proposed WDLQ-based AFC achieves a fast adaptive frequency calibration in less than 25 μs with 10 MHz reference clock.

II. CONFIGURATIONS

A. Wide-band frequency synthesizer

The block diagram of wide-band frequency synthesizer is shown in Fig. 1. The synthesizer consists of a reference divider, a programmable main divider, a phase frequency detector (PFD), a charge pump, a wide-band VCO, a loop filter, a serial bus interface block and an adaptive frequency calibration (AFC) block.

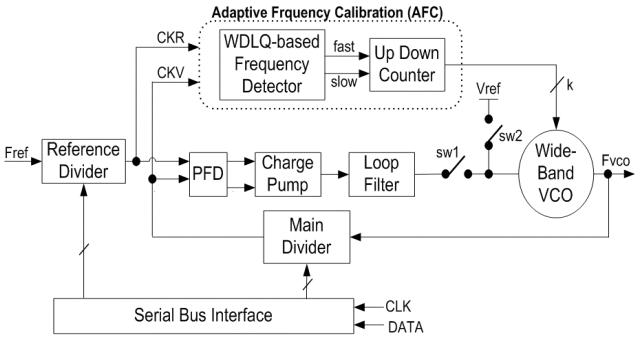

Figure 1. Block diagram of wide-band frequency synthesizer.

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Each time the frequency synthesizer is programmed via a serial bus interface, the AFC block is enabled to select the proper transfer curve among the many curves of the VCO. In this mode, switch 1 (sw1) is open and switch 2 (sw2) is closed to the reference voltage (V_{ref}) to make the VCO operate at the center of its transfer curve during the AFC operation. After fixing the code for selecting the bank of VCO, switch 1 (sw1) is closed and switch 2 (sw2) is open to settle the VCO phase by using the closed loop of the PFD, charge pump and loop filter instead of the AFC block.

The total lock time of the frequency synthesizer, which is the sum of AFC operation time and normal PLL lock time, can be shortened by the fast response AFC as well as the wide PLL loop bandwidth. The adaptive PLL loop bandwidth control can help to lower the lock time, but the loop gain control for wide-band operation may cause stability problem. However, the fast and accurate AFC can shorten the total lock time in wide-band applications apart from PLL loop characteristics.

B. *Wide-band VCO and AFC*

The specified wide-band VCO tuning range is 1 GHz (50 %) from 1.5 to 2.5 GHz, which meets the requirements of most modern wireless transceivers. The VCO gain (K_{vco}) is 20 MHz/V, frequency resolution (F_{res}) is 20 MHz, and binary weighted 6-bit switched-capacitors bank LC tank is used to cover the whole range as shown in Fig. 2. Overlap between the adjacent transfer curves is desired feature for design margin.

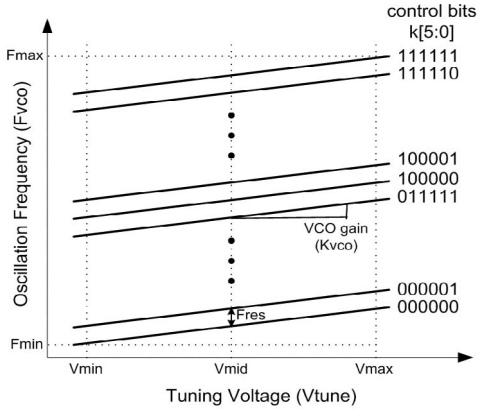


Figure 2. Transfer curves of the specified VCO with control bits.

The number of control bits generated by the AFC can be expressed by (1), and the AFC output code is used for VCO bank selection.

$$K \geq \log_2\left(\frac{F_{band}}{F_{res}}\right) = \log_2\left(\frac{2.5-1.5GHz}{20MHz}\right) = 5.64 \qquad (1)$$

The essential function of the AFC is to determine the oscillation frequency is faster or slower than the desired VCO frequency, and generate the code for the target bank. The next section de-scribes the wide-range frequency detection scheme and implementation of the proposed AFC.

III. IMPLEMENTATION OF AFC

A. *Digital quadricorrelator*

A digital quadricorrelator whose operation is based on Teager's analog energy tracker can be derived as Fig. 3 [4]. Since the output of the quadricorrelator is proportional to the square of the offset of the input signal, the circuit can be used to detect the frequency offset of the input signal and the VCO signal.

The outputs of a pair of the low-pass filters are quantized by limiters (sgn) and multiplied by binary operation, and delay-difference circuits are used for differentiator implementation. Assuming perfect multipliers and low-pass filters, the quantized in-phase and quadrature outputs are calculated to be

$$\begin{aligned}\hat{V}_1(t) &= \mathrm{sgn}\left\{\left(\frac{d}{dt}X_I(t)\right)\Delta\omega\, X_Q(t)\right\} \\ &= \mathrm{sgn}\left(\frac{d}{dt}X_I(t)\right)\mathrm{sgn}(\Delta\omega)\,\mathrm{sgn}\left(X_Q(t)\right)\end{aligned} \qquad (2)$$

$$\begin{aligned}\hat{V}_2(t) &= \mathrm{sgn}\left\{X_I(t)\Delta\omega\left(\frac{d}{dt}X_Q(t)\right)\right\} \\ &= \mathrm{sgn}\left(X_I(t)\right)\mathrm{sgn}(\Delta\omega)\,\mathrm{sgn}\left(\frac{d}{dt}X_Q(t)\right)\end{aligned} \qquad (3)$$

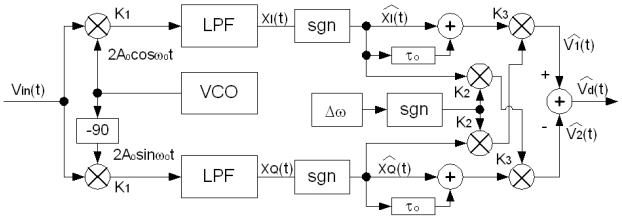


Figure 3. Block diagram of digital quadricorrelator.

B. *Digital logic quadricorrelator*

A configuration of a digital logic quadricorrelator (DLQ) based on Fig. 3 is shown in Fig. 4. The DLQ consists of two D flip-flops (FF1,3) as a pair of mixer (K1) with a LPF, two flip-flops (FF2,4) followed by two AND-gates (AND1,2) as a pair of differentiators, two AND-gates (AND3,4) as multipliers (K2, K3), and an OR-gate (OR1) as a summer. The operations of the DLQ will be considered for three different cases.

Case 1 ($\omega_i = \omega_o$): If the input frequency is equal to the VCO clock frequency, the outputs of FF1,3 (A,A',C,C') are always "1" or "0" determined by its initial phase. As the output of AND1,2 is always "0", the output of AND3,4 (V_1 ,V_2) is always "0". It is very important and critical to be recognized that the DLTD produces no spurious output when the frequency offset is zero.

Case 2 ($\omega_i < \omega_o$): If the input frequency is lower than the clock frequency, (A,A') ports produce square waves, which

have the frequency component of the frequency offset. (C,C') ports give 90˚delayed versions of the waves from the (A,A') ports. AND1 delivers a rising edge differentiation of (A,A') ports' outputs. After combining (C,C') ports' states, the output of AND3 (V_1) produces one clock width "1" pulses, whereas the V_2 port remains to be "0" state. The "1" pulses from V_1 port means that the VCO frequency is higher than the input frequency. The number of "1" pulses for a specific time period is proportional to the magnitude of the frequency offset.

Case 3 ($\omega_i > \omega_o$): If the input frequency is higher than the clock frequency, the V_2 port delivers "1" pulses, whereas the V_1 port remains to be "0" state.

From previous considerations, V1 signal can be used for indicating the VCO frequency is faster than the reference clock rate, and V2 signal for indicating the VCO frequency is slower. The simulation results show that the DLQ has a linear frequency discrimination characteristic of ±20 % of clock rate. For wide-range applications, the discrimination range can be extended with wide-range DLQ (WDLQ) [5].

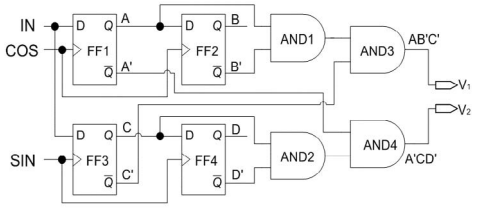


Figure 4. Configuration of digital logic quadricorrelator.

C. Wide-range DLQ (WDLQ)

A configuration of a wide-range DLQ (WDLQ) is shown in Fig. 5. Front-end D-FFs (FF1,3) in Fig. 4 are replaced by a wide-range mixers as shown in Fig. 6.

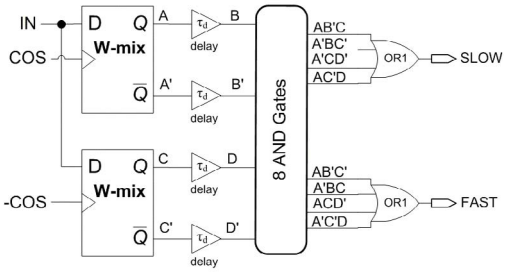


Figure 5. Configuration of wide-range DLQ. (WDLQ)

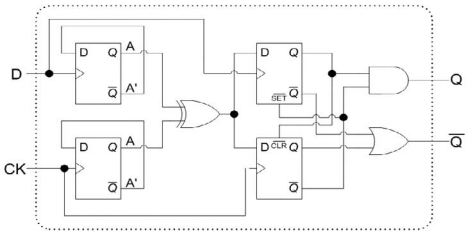


Figure 6. Configuration of wide-range mixer.

By summing four AND gate outputs, we can increase the FD gain. The WDLQ detects the direction and magnitude of oscillation frequency offset up to ±100 % of the clock rate. Fig. 7 shows simulated frequency discrimination characteristics of DLQ and WDLQ.

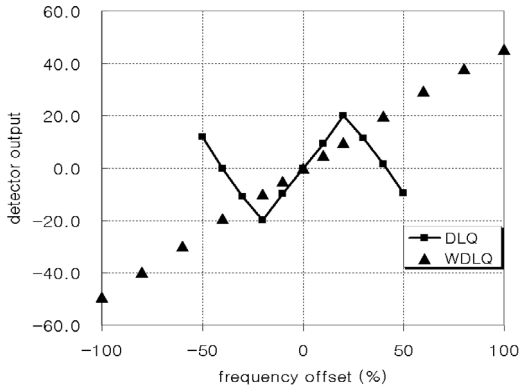


Figure 7. Frequency discrimination characteristics for DLQ and WDLQ.

D. Implementation of WDLQ-based AFC

The proposed AFC block which is based on the wide-band digital logic quadricorrelator (WDLQ) is shown in Fig. 8.

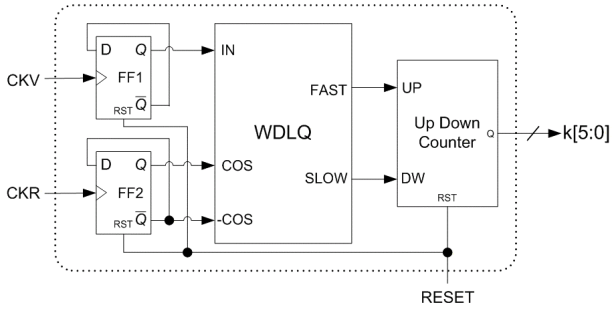


Figure 8. Block diagram of WDLQ-based AFC.

Front-end D-FFs (FF1,2) are used to make the CKV and CKR signals have 50 % duty cycle, which is desired for proper WDLQ operation. The up-down counter uses a pulse on the FAST port as an up count signal and a pulse on the SLOW port as a down count signal, and completes the code value k[5:0] to select the proper bank frequency. Table I shows the AFC codes for the selected bank frequencies.

TABLE I. AFC CODES FOR THE SELECTED BANK FREQUENCIES

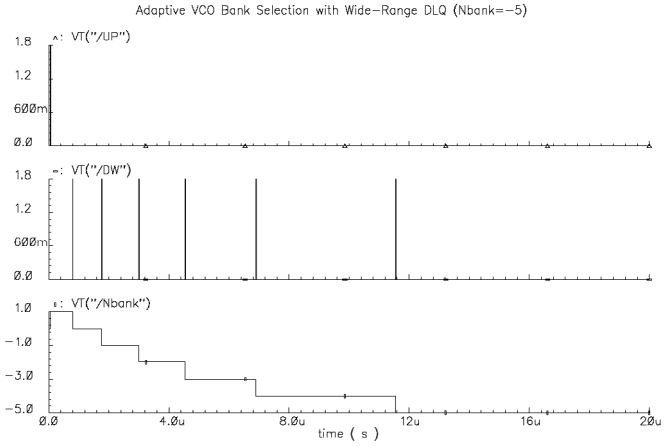
Fbank [MHz]	Nbank	k	k[5:0]	Foffset [%]
1500	−25	7	000111	−25
1520	−24	8	001000	−24
1960	−2	30	011110	−2
1980	−1	31	011111	−1
2000	0	32	100000	0
2020	1	33	100001	1
2040	2	34	100010	2
2480	24	56	111000	24
2500	25	57	111001	25

IV. SIMULATION RESULTS

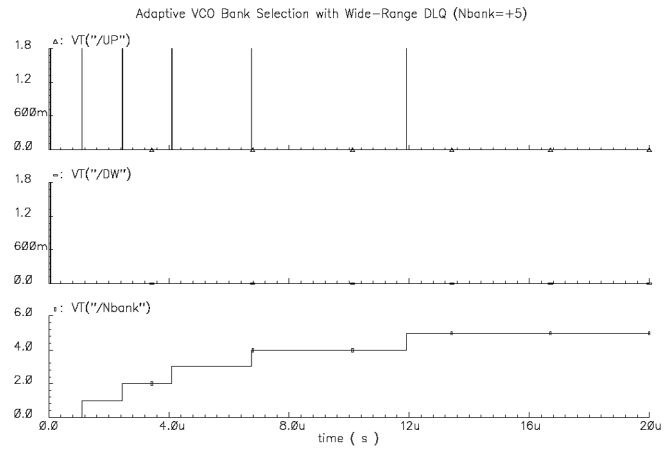
The CADENCE Spectre simulation results of the proposed AFC technique with the variations of the N_{bank} value are shown in Fig. 9(a)~(c). The pulses on the down port (DW) finalize the N_{bank} value down to -5 in Fig. 9(a), and the pulses on the up port (UP) finalize the N_{bank} value up to +5 in Fig. 9(b). F_{bank}, k, and F_{offset} can be expressed by (4).

$$F_{bank} = F_0 + F_{res} \times N_{bank} = 2GHz + 20MHz \times N_{bank}$$
$$k = N_{bank} + 32 \qquad (4)$$
$$F_{offset=} \frac{F_{bank} - F_0}{F_0} \times 100 = \frac{F_{bank} - 2GHz}{2GHz} \times 100 \quad [\%]$$

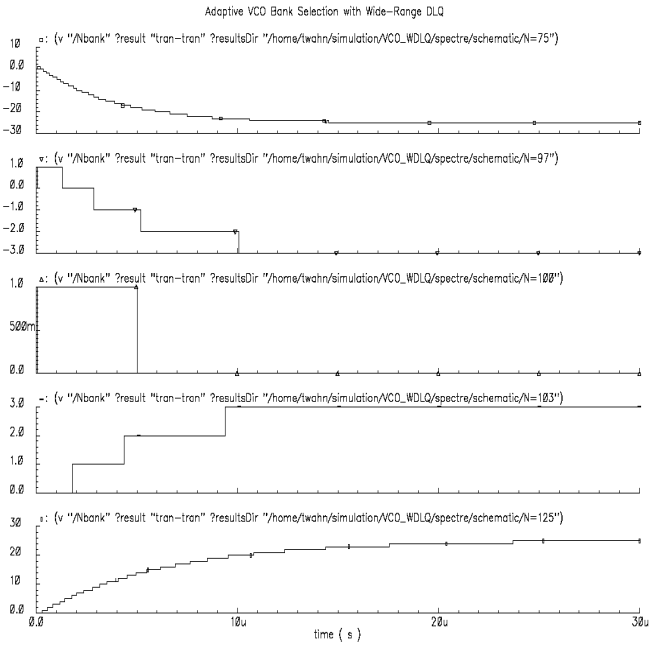
Fig. 9(c) shows the N_{bank} value decision for the five selected cases. The bank frequency of 1.5 GHz is selected when the N_{bank} value is -25, 2.0 GHz is selected when the N_{bank} value is 0, and 2.5 GHz is selected when the N_{bank} value is +25 as in Table 1. The proposed WDLQ-based AFC achieves a fast adaptive frequency calibration in less than 25 μs with 10 MHz reference clock for the specified VCO tuning range is as wide as 1 GHz (50 %) from 1.5 to 2.5 GHz.



(a) N_{bank} = -5. (F_{bank} = 1900 MHz, k = 27, F_{offset} = -5 %)



(b) N_{bank} = +5. (F_{bank} = 2100 MHz, k = 37, F_{offset} = +5 %)



(c) N_{bank} = -25, -3, 0, +3, and +25.

Figure 9. Simulation results of the proposed AFC.
(a) N_{bank} = -5. (b) N_{bank} = +5. (c) N_{bank} = -25, -3, 0, +3, and +25.

V. CONCLUSION

In this paper, a fast response adaptive frequency calibration (AFC) technique for wide-band frequency synthesizers is presented. In order to operate in a wide-band frequency range, a wide-range digital logic quadricorrelator (WDLQ) is proposed for frequency detector. The CADENCE Spectre simulation results show that the WDLQ-based AFC achieves a fast adaptive frequency calibration in less than 25 μs with 10 MHz reference clock, which is shortened by half in comparison with the previous works.

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