A New Design Methodology for Reconfigurable Sigma-Delta Modulator for Fractional Frequency Synthesizer

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I. Introduction

Frequency synthesizer has been developed to support various communication systems in recent wireless communication systems. Consequently, the design of frequency synthesizer which is suitable for high performance communication system is essential, and frequentcy synthesizer must maintain low phase noise. The design of VCO and fractional divider is important in frequency synthesizer which is based on PLL. Specially, sigma-delta modulator is one of important design blocks when fractional frequency synthesizer is integrated in low noise system. But, the design methodology which is accurate for sigma-delta modulator in fractional frequency synthesizer is not shown in most designs. Also, the needs of reconfigurable sigma-delta modulator for low noise characteristics supporting other frequencies is increasing nowadays. In this paper, the 3rd-order reconfigurable serial single stage sigma-delta modulator using a new design methodology is proposed and verified.

II. Design of the Reconfigurable Sigma-Delta Modulator

Fig.1 shows the block diagram of fractional frequency synthesizer. The fractional frequency synthesizer has PFD, CP, LF, VCO, divider, and SDM (sigma-delta modulator) that determines fractional division ratio [1]. The design of SDM is possible with the method which is shown in Fig.2. This paper proposes the design and verification methods of SDM using Simulink (MATLAB), ModelSim, and HSPICE.

At first, when the specification of the frequency synthesizer is decided, the design method and performance of SDM is determined. And then the filter equation that is used to design SDM is fixed according to the SDM specification [2]. The noise transfer function (NTF) of SDM filter in this paper is obtained as

$$H_{NTF}(z) = \frac{z^3 - 3z^2 + 3z - 1}{z^3 - 1.162z^2 + 0.6959z - 0.1378} \quad (1)$$

As shown in Fig. 3-(a), the finalized filter equation decides coefficients of behavior block that consists of functional blocks in Simulink. The design of SDM is continued until SDM satisfies the specification. Then, the SDM is implemented by logic blocks that consists of adder, accumulator, switch, and so on for ModelSim block diagram as shown in Fig. 3-(b). The design of digital logic block is possible with VHDL or Verilog and simulated by HDL code in ModelSim. The SDM that consists of VHDL or Verilog code generates digital waveform in result. But, the result of the ModelSim simulation is difficult to check the desired frequency characteristics. But the proposed ModelSim-Simulink co-simulation using ModelSim simulation results could confirm the desired SDM frequency characteristics easily. Fig. 4 shows the results of ModelSim-Simulink co-simulation. Co-simulation is continued until it satisfies the frequency characteristic of the SDM.

The logic blocks of verified SDM using ModelSim could be designed in circuit level. As shown in Fig. 5, if the results of Simulink, ModelSim, and HSPICE are equal, the SDM implemented in circuit level has the same frequency characteristics. So it is possible to layout the designed digital blocks directly, as shown in Fig. 6. If the SDM for other frequency synthesis is needed, the parameters could be changed easily by using the original layout. The proposed reconfigurable switch block could be modified without difficulty, so it could shorten the system development time. The reconfigurable switch block is comprised of inverters and buffers. The coefficients of the reconfigurable switch block is decided by the layout connection changes of inverter and buffer logic.

III. Conclusion

The reconfigurable sigma-delta modulator for fractional frequency synthesizer was designed with Simulink and ModelSim co-simulation method, and can verify the desired sigma-delta modulator frequency characteristics easily. Also, the change of SDM coefficients is done by the reconfigurable switch block, so system development time could be reduced. And the proposed methodology and architecture are expected to improve SDM flexibility and design time.

ACKNOWLEDGMENT

This work was sponsored by ETRI SoC Industry Promo-tion Center, Human Resource Development Project for IT SoC Architect. CAD Tools are supported by IDEC.

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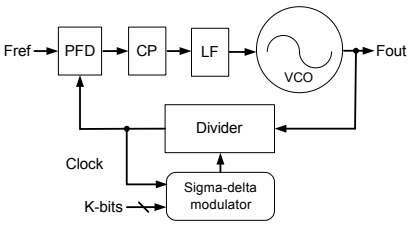


Fig. 1. Block diagram of the fractional frequency synthesizer

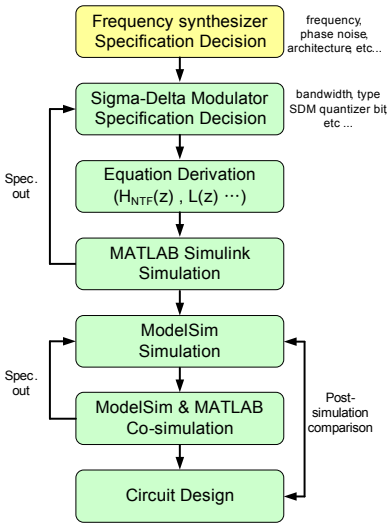
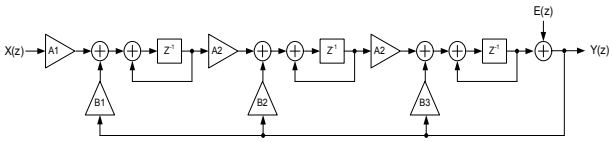
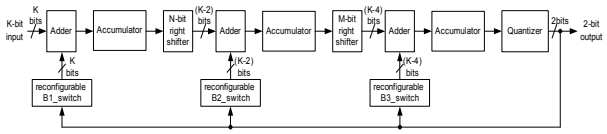


Fig. 2. Flow chart of sigma-delta modulator design method



(a) MATLAB Simulink implementation



(b) ModelSim implementation

Fig. 3. The relation between block diagrams

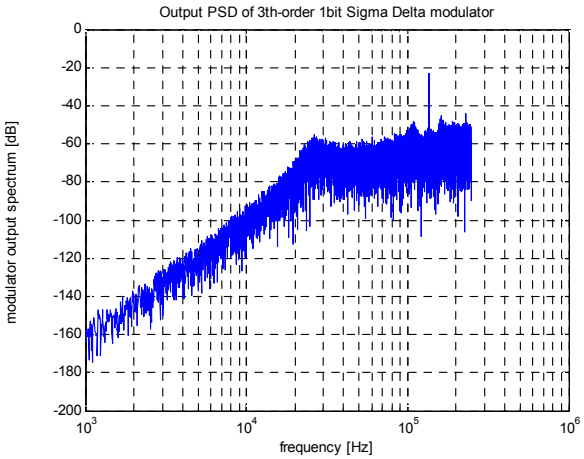


Fig. 4. Noise shaping results by MATLAB Simulink-ModelSim co-simulation

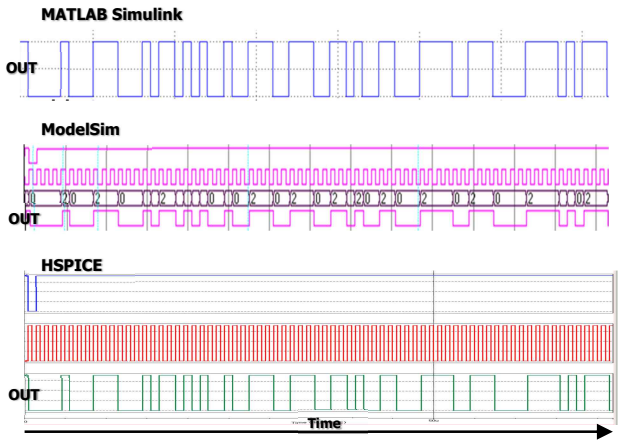


Fig. 5. Comparision of MATLAB Simulink, ModelSim and HSPICE simulation

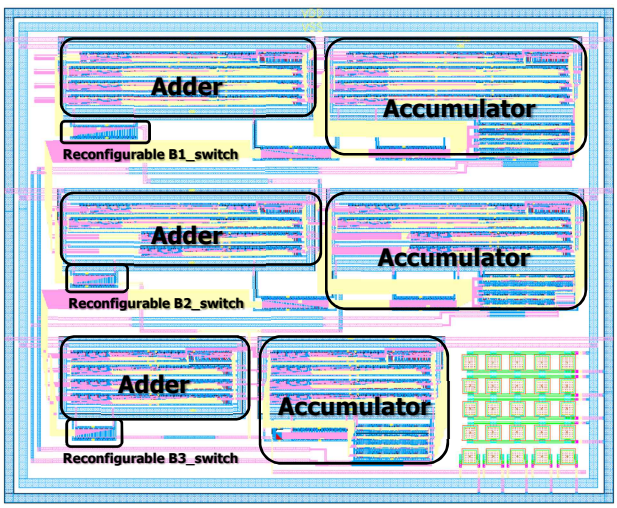


Fig. 6. Layout of the proposed reconfigurable SDM