

A 0.94–2.3-GHz Frequency Synthesizer with Low VCO Gain Variation and Calibration for Uniform VCO Frequency Interval

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Abstract - A Σ - Δ fractional-N frequency synthesizer featuring wide and multi-band, low VCO-gain (K_{VCO}) variation and uniform VCO frequency interval is presented. 5-bit switched capacitor bank LC VCO is used to cover wide and multi-band frequency operation for mobile-DTV (Digital Television) applications, and switched varactor bank and VCO frequency interval calibration block are added to conventional capacitor bank scheme for low K_{VCO} variation and uniform VCO frequency interval. The VCO tuning range is as wide as 1360 MHz (59%) from 940 MHz to 2.3 GHz in 64 channels and the K_{VCO} is reduced by one-third in comparison with the previous works which used conventional method. The proposed synthesizer consumes 18 mW from a single 1.8-V supply voltage and VCO phase noise is lower than -100 dBc/Hz at 1MHz offset for 1 GHz, 1.5 GHz, and 2 GHz output frequency.

Keywords: Wide and multi-band VCO, VCO gain variation, varactor, calibration.

1 Introduction

Recently, the system has been integrated by various technology according to communication and semiconductor development. Specially, mobile multimedia system could be used anytime and anywhere has improved rapidly. First of all, mobile-DTV has been serviced many specifications, and popular mobile-DTV specifications are DVB-H, ISDB-T and T-DMB.

Modern mobile-DTV systems need a wide and multi-band frequency synthesizer to provide various local oscillation signals for a cost-effective RFIC that supports DVB-H, ISDB-T, and DMB [1]. The wide and multi-band and low phase-noise VCO (voltage-controlled oscillator) is a key component for wide tuning features which are in high demand by multi-band and multi-mode applications.

A general method for wide frequency band is to use the switched capacitor bank LC VCO. However, K_{VCO} of low oscillation frequency in VCO is decreased for high oscillation frequency because capacitor switch value of

VCO is decided to oscillation frequency in generally. Thereby K_{VCO} is fluctuated by frequency selection bit and is decreased by the capacitance increment of VCO. Therefore K_{VCO} variation is the drawback of wide, and multi-band frequency synthesizer, and it degraded the total performance of communication systems [2]. To maintain low K_{VCO} variation and support wide and multi-band frequency range, we propose additional switched varactor banks and a VCO frequency calibration block to conventional capacitor bank scheme.

In this paper, an integrated Σ - Δ fractional-N frequency synthesizer (FNFS) except LF(loop filter) with switched varactor bank and VCO frequency calibration block to conventional 5-bit switched capacitor bank and 1-bit switched inductor bank LC VCO configuration is implemented with 0.18- μ m CMOS technology. The tuning range of the designed FNFS is as wide as 1360 MHz (59%) from 940 MHz to 2.3 GHz, which can cover all the desired frequencies for the DVB-H/ISDB-T/T-DMB specifications and oscillation frequency decrement to process variation. The designed FNFS achieves about 30% smaller K_{VCO} variation than that of a conventional design. Moreover, because the additional switched varactor bank and VCO frequency calibration block do not need additional input bit and input current, it is well suited to low-power-consumption mobile-DTV applications. The designed FNFS consumes 18mW from a single 1.8-V supply voltage and VCO phase noise is lower than -100 dBc/Hz at 1MHz offset for 1 GHz, 1.5 GHz, and 2 GHz output frequency.

2 FNFS architecture

A block diagram of the proposed wide and multi-band FNFS is illustrated in Figure 1. The frequency synthesizer consists of a reference counter, a PFD (phase frequency detector), a CP (charge-pump), a LF, a wide-band VCO, a prescaler, a main divider, and a SDM (Σ - Δ modulator). Dead-zone free PFD and charge-pump are used to reduce in-band phase noise, which is caused mainly by the folding-in noise of the SDM when PFD and charge-pump operates around non-linear region.

Divider consists of a prescaler, a main divider, and a SDM. Prescaler is SCL type and determines FNFS output frequency at high frequency operation of VCO. Main divider is programmable counter type N-divider. The 1-bit 3rd order SDM with 2-level quantizer with multiple feedback paths is used, where each stage consists of an adder, an accumulator, and a multiplier for the dynamic scaling.

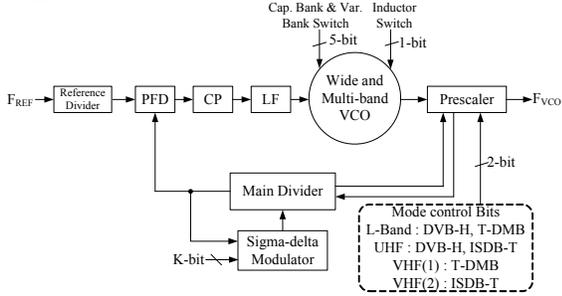


Figure 1. Block diagram of the wide and multi-band FNFS

To cover wide frequency band of about 1360MHz with the small VCO gain and supply voltage of 1.8-V, the integrated VCO has 64 VCO curves by using 5-bit switched capacitor bank and 1bit inductor switch. The frequency range of VCO is specified as the range from 940 MHz to 2.3 GHz which meets the requirements of the DVB-H/ISDB-T/T-DMB receiver as summarized in Table 1.

TABLE 1. FREQUENCY SPECIFICATIONS FOR MOBILE-DTV

DTV Spec.	Frequency range [MHz]
DVB-H	470 ~ 890 (UHF), 1452-1675 (L-Band)
ISDB-T	90 ~ 222 (VHF), 470 ~ 770 (UHF)
T-DMB	174 ~ 216 (VHF), 1450 ~ 1492 (L-Band)

3 Wide and multi-band VCO design

Figure 2 shows a proposed LC VCO design. VCO is designed by PMOS core for low phase noise. The proposed VCO is composed of switched capacitor bank that is used to a conventional VCO, a switched inductor, the proposed switched varactor bank, and the VCO frequency calibration block for wide frequency range.

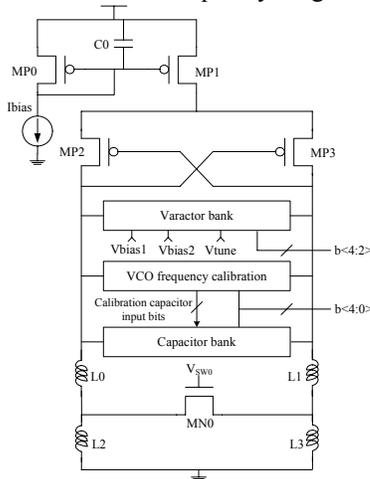


Figure 2. Block diagram of the proposed wide-band VCO

Conventional switched capacitor bank LC VCO design is widely used to achieve reduced VCO phase noise as well as wide frequency band, and Figure 3(a) shows the ideal VCO tuning characteristics. However, the linearity and uniformity of the frequency-voltage gain characteristics can be deteriorated as oscillation frequency range is increased, because the oscillation frequency (f_{VCO}) is described as equation (1). Actually K_{VCO} becomes larger for the higher frequency band and smaller for the lower frequency band with a conventional switched-capacitor bank scheme as shown in Figure 3(b).

$$f_{VCO} = \frac{1}{2\pi \sqrt{L \left(\frac{C_v C_b}{C_v + C_b} + \sum_{i=1}^K C_u + C_p \right)}} \quad (1)$$

C_u : unit capacitance of capacitor bank
 C_p : parasitic capacitance

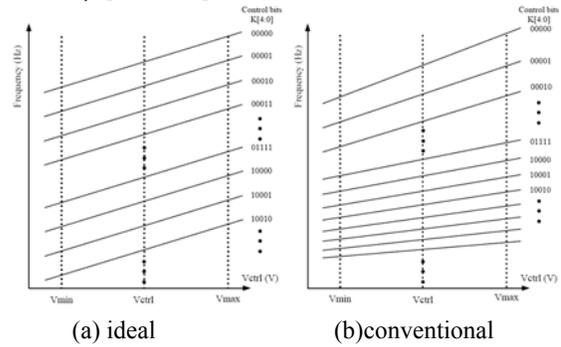


Figure 3. Block diagram of the wide-band FNFS

K_{VCO} variation degrades the performance of the PLL, so it must be suppressed when wide frequency range is necessary. Moreover, the current of charge pump must be changed with K_{VCO} to attain constant PLL loop gain for stable operation [3]. To maintain low K_{VCO} variation, the proposed low K_{VCO} variation technique using switched varactor bank and K_{VCO} frequency calibration is described in next section.

4 Low K_{VCO} Variation Technique

4.1 Switched Varactor Bank

To suppress K_{VCO} variation for wide and multi-band VCO design, we introduce the switched varactor bank in Figure 4. The switched varactor bank consists of two voltage biasing varactor blocks that each voltage biasing block has three varactor switch blocks. Switched varactor block biases that improve varactor capacitance characteristics are minimized as two. To get low K_{VCO} variation, total capacitance fluctuation of switched varactor bank is maintained by on/off operation of varactor switch. Input of switched varactor bank uses some signal of capacitor bank to avoid additional control input. In this work, input bit of switched varactor bank is 3-bit of switched capacitor bank from MSB. The figure of varactor switch bit is determined by total capacitor bank input bit of VCO.

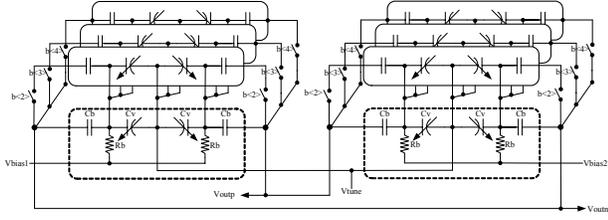


Figure 4. Proposed switched varactor bank configuration

In this paper, a conventional 5-bit capacitor-bank type VCO is compared for the feasibility check of the proposed K_{VCO} suppression technique, and the target frequency band of VCO is specified as the range from 940 MHz to 2.3 GHz which meets the requirements of the DVB-H/ISDB-T/T-DMB receiver. Figure 5 shows the simulated frequency voltage gain curve distribution of the conventional and proposed VCOs. Each VCO exhibited 64 frequency curves by inductor switching and setting $b<4:0>$ to control the total capacitance of the switched-capacitor banks. As illustrated in Figure 5 and Table 2, the proposed K_{VCO} variation is decreased $\pm 27.7\%$ when output frequency band is high when inductor switch turns on and $\pm 30.3\%$ when output frequency band is high by which inductor switch turns off.

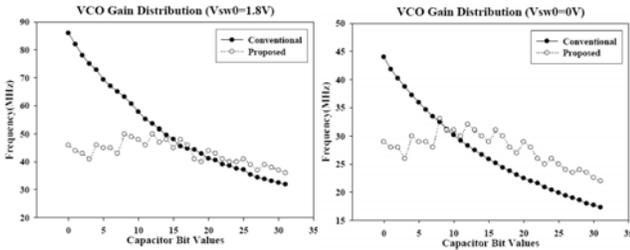


Figure 5. VCO gain distribution

TABLE 2. SUMMARY OF K_{VCO} CHARACTERISTICS

High Frequency Band ($V_{SW0}=1.8V$)		
	Conventional	Proposed
K_{vco} Max.	86.1 MHz/V	46.0 MHz/V
K_{vco} Min.	37.1 MHz/V	36.1 MHz/V
K_{vco} Variation	$\pm 39.8\%$	$\pm 12.1\%$
Low Frequency Band ($V_{SW0}=0V$)		
	Conventional	Proposed
K_{vco} Max.	44.2 MHz/V	29.2 MHz/V
K_{vco} Min.	17.3 MHz/V	22.3 MHz/V
K_{vco} Variation	$\pm 43.7\%$	$\pm 13.4\%$

4.2 VCO Frequency Calibration

The switched varactor bank improves VCO gain fluctuation, but intervals of VCO frequency couldn't be improved. When only switched varactor bank is used, total oscillation frequency range is similar to the output frequency range of conventional VCO. So we propose VCO frequency interval calibration block as in Figure 6. The VCO frequency interval calibration block is comprised of VCO frequency interval calibration logic and

calibration capacitor bank, which uses capacitor bank input without additional control input bit.

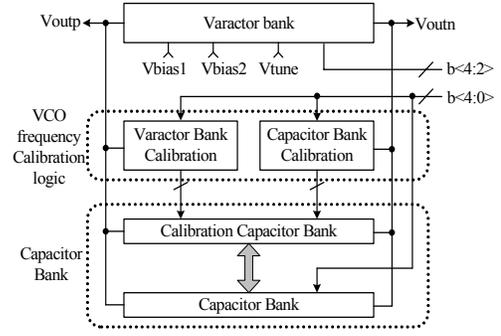


Figure 6. Total tuning block with VCO frequency calibration

VCO frequency interval calibration logic consists of digital logics includes varactor bank calibration logic and capacitor calibration logic, and the oscillation frequency is tuned by two calibration logics which is operated by calibration capacitor bank. This logic is similar to thermometer decoder and minimizes additional capacitor value for layout size efficiency. And total frequency tuning block (varactor, capacitor, calibration block) operation is distinguished each other for low power consumption, as illustrated in Table 3.

TABLE 3. OPERATIONS OF TOTAL VCO TUNING BLOCKS

Binary values of capacitor bank	Capacitor bank	Varactor bank	Varactor bank calibration	Capacitor bank calibration
00000 – 00011	○	×	×	×
00100, 01000, 01100, 10000, 10100, 11100	○	○	○	×
otherwise	○	○	○	○

Figure 7 shows post simulation results of VCO frequency versus control voltage using LPE (Layout Parasitic Extraction). VCO frequency interval is improved by calibration block for conventional VCO. This uniform VCO frequency interval calibration extends VCO oscillation frequency range, and could apply to automatic frequency calibration and wide-range digital logic quadrice correlator for fast settling technique [4].

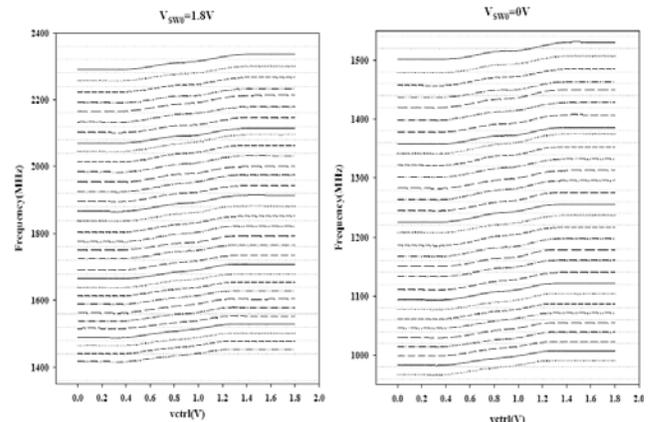


Figure 7. VCO frequency vs. control voltage curves

5 FNFS DESIGN

There are many kinds of Σ - Δ modulator (SDM) schemes, and we used the 3rd-order reconfigure-able sigma-delta modulator SDM for phase noise shaping, and a 1-bit quantizer architecture for simple and stable operation. The 3rd-order single stage SDM consists of three accumulators and six coefficients. The design was verified with Simulink and ModelSim co-simulation method. Figure 8 shows the phase noise and post simulation results of the designed SDM.

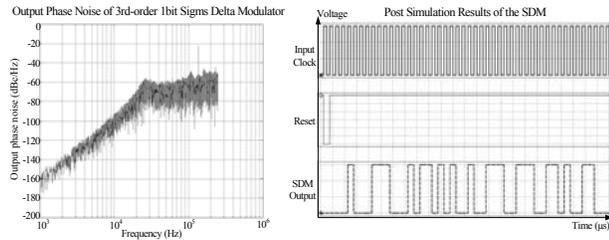


Figure 8. SDM simulation results

Figure 9 shows the layout of the proposed FNFS, which occupies the area of $2700 \mu\text{m} \times 2100 \mu\text{m}$. The VCO layout is arranged as symmetrical as possible and all capacitors and transistors are placed nearby, so energy loss due to connection wires can be minimized. Figure 10 shows post simulation results of designed divider using VCO output.

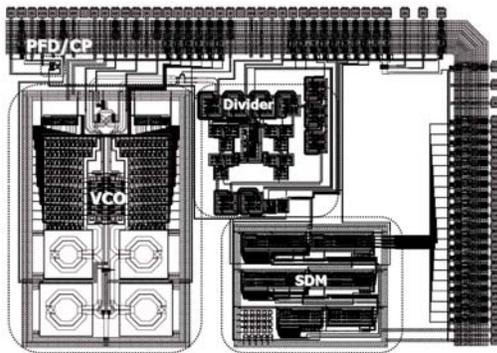
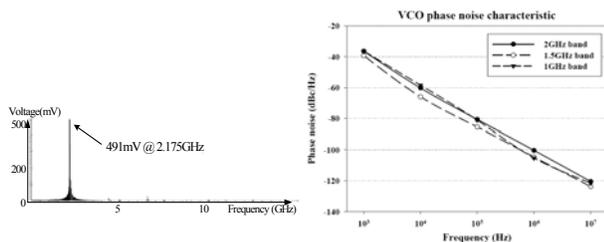
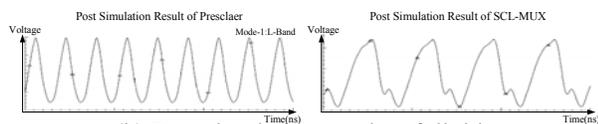


Figure 9. Layout of the designed FNFS



(a) Post simulation results of VCO



(b) Post simulation results of divider

Figure 10. VCO and divider post simulation results

6 Conclusions

In this paper, the integrated wide and multi-band FNFS with low K_{VCO} variation and uniform VCO frequency interval technique is presented. The designed FNFS consumes 18 mW from a single 1.8 V supply voltage and VCO phase noise is lower than -100 dBc/Hz at 1MHz offset for 1 GHz, 1.5 GHz, and 2 GHz output frequency. The VCO tuning range is as wide as 1360 MHz (59%) from 940 MHz to 2.3 GHz in 64 channels, which can cover all the desired frequencies for DVB-H/ISDB-T/T-DMB receivers. By adding proposed switched varactor bank and VCO frequency interval calibration block to conventional 5-bit switched capacitor bank LC VCO configuration, we achieve 30% smaller K_{VCO} fluctuation than that of a conventional design. Because the proposed FNFS has the suppressed low VCO gain variation and uniform VCO frequency interval while maintaining wide tuning range without additional bias current and input port at low cost, and it is well suited for multi-band and multi-mode mobile applications.

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References

- [1] Patrick Antoine et al., "A direct-conversion receiver for DVB-H," IEEE Journal of Solid State Circuits, vol. 40, pp.2536-2546, Dec. 2006.
- [2] Donhee H. and Hajimiri, A., "Design and optimization of a low noise 2.4GHz CMOS VCO with integrated LC tank and MOSCAP tuning," ISCAS 2000 - IEEE International Symposium on Circuits and Systems, vol. 1, pp.331-334, May 2000.
- [3] Eun-Yung Sung et al., "A Wideband 0.18- μm CMOS Fractional-N Frequency Synthesizer with a single VCO for DVB-T," Asian Solid-State Circuits Conference, Nov. 2005.
- [4] Yoon, C., et al., "A Fast Response Digital Logic Tone Detector," 2005 IEEE INTERNATIONAL MIDWEST SYMPOSIUM ON CIRCUITS AND SYSTEMS, vol. 1, pp.239-242, Aug. 2005.