A Fractional-N Frequency Synthesizer with a Wide-band Small Gain-Fluctuation VCO for Mobile DTV Applications

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Abstract

A fully integrated Σ-Δ fractional-N frequency synthesizer featuring wide-band and small VCO-gain (K_{VCO}) fluctuation is presented. To cover wide-band frequency operation for mobile DTV applications, 6-bit switched-capacitor bank LC VCO is used, and for small K_{VCO} fluctuation, four self-controlled varactor blocks are added to conventional capacitor bank scheme. The integrated VCO tuning range is as wide as 890 MHz (65%) from 910 MHz to 1.8 GHz, which can cover all the desired frequencies for the DVB-H/ISDB-T/T-DMB receiver and achieves 52% smaller K_{VCO} fluctuation than that of a conventional design.

1. Introduction

Modern mobile DTV systems need a wide-band frequency synthesizer to provide various local oscillation signals for a cost-effective RFIC that supports DVB-H, ISDB-T, and DMB [1]. The wide-band and low phase-noise voltage-controlled oscillator (VCO) is a key component for wide tuning features which are in high demand by the multi-band multi-mode applications [2].
A general method for both reduced VCO gain (K_{VCO}) and wide frequency band is to use the switched-capacitor bank LC VCO [3]. However, K_{VCO} fluctuates widely in the wide oscillation frequency range of the VCO, thereby degrading the performance of the PLL-based frequency synthesizer [4]. To suppress VCO gain-fluctuation while maintaining wide frequency range and without degrading phase noise, we propose additional self-controlled varactor blocks to conventional capacitor bank scheme.
In this paper, a fully integrated Σ-Δ fractional-N frequency synthesizer (FNFS) with four self-controlled varactor blocks to conventional 6-bit switched-capacitor bank LC VCO configuration is implemented with 0.18-μm CMOS technology. The tuning range of the designed FNFS is as wide as 890 MHz (65%) from 910 MHz to 1.8 GHz, which can cover all the desired frequencies for the DVB-H/ISDB-T/T-DMB receiver and achieves 52% smaller K_{VCO} fluctuation than that of a conventional design. Moreover, because the additional self-controlled varactor blocks do not need additional bias current, it is well suited to low power mobile DTV applications. The Σ-Δ modulator for fractional frequency synthesizer is designed with MATLAB Simulink and ModelSim co-simulation method. The designed FNFS consumes 11.4 mA from a single 1.8 V supply voltage and the experimental results show -80 dBc/Hz in-band phase noise and -127 dBc/Hz out-of-band phase noise at 1 MHz-offset frequency.

2. Implementation of a Wide-band FNFS

A block diagram of a proposed fully integrated wide-band FNFS is illustrated in Figure 1. The frequency synthesizer consists of a reference counter, a phase frequency detector (PFD), a charge-pump, a wide-band VCO, a dual modulus prescaler, a programmable counter, a Σ-Δ modulator (SDM), and a loop filter.

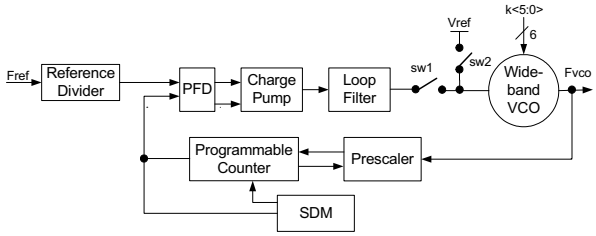

Figure 1. Block diagram of a wide-band FNFS

Dead-zone free PFD and charge-pump are used to reduce the in-band phase noise, which is caused mainly by the folding-in noise of the SDM when PFD and charge-pump operates around non-linear region.
Main divider consists of a dual-modulus prescaler, a SDM and a programmable counter. Dual modulus prescaler operates at high frequency of VCO and is SCL type. The 1-bit 3rd order SDM with a 2-level quantizer with multiple feedback paths is used, where each stage consists of an adder, an accumulator, and a multiplier for the dynamic scaling .
To cover wide frequency band of almost 900MHz with a small VCO gain and a small supply voltage of 1.8-V, the integrated VCO has 64 VCO curves by using 6-bit switched capacitor bank. The frequency range of VCO is specified as the range from 890 MHz to 1.8 GHz which meets the requirements of the DVB-H/ISDB-T/T-DMB receiver as summarized in Table 1.

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Table 1. Frequency specifications for mobile DTV

DTV Spec.	Frequency range [MHz]
DVB-H(UHF)	470～890
DVB-H(L-Band)	1452～1492
DVB-H(US)	1670～1675
ISDB-T(UHF)	470～770
T-DMB(L-Band)	1450～1492

3. Wide-band VCO Design

Figure 2 shows a conventional switched-capacitor bank LC VCO design which is widely used to achieve reduced VCO phase noise as well as wide frequency band, and Figure 3(a) shows the ideal VCO tuning characteristics. However, because the oscillation frequency (f_{VCO}) is described as equation (1), the linearity and uniformity of the frequency-voltage gain characteristics can be deteriorated as the oscillation frequency range is increased. Actually K_{VCO} becomes larger for the higher frequency band and smaller for the lower frequency band with a conventional switched-capacitor bank scheme as shown in Figure 3(b).

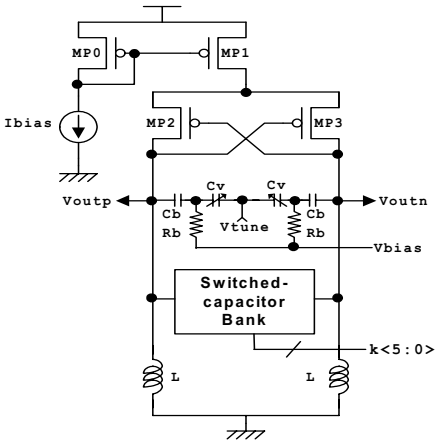
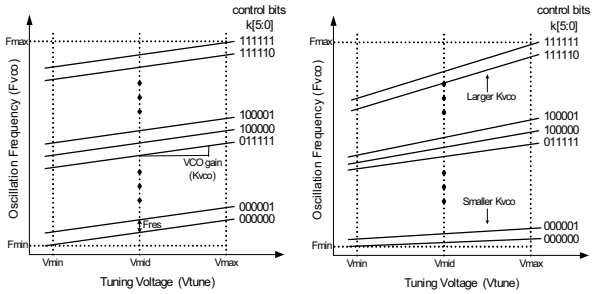


Figure 2. Conventional switched-capacitor bank VCO

$$f_{VCO} = \frac{1}{2\pi\sqrt{L\left(\frac{C_v C_b}{C_v + C_b} + \sum_{i=1}^{K} C_u + C_p\right)}} \quad (1)$$

C_u : unit capacitance of capacitor bank
C_p : parasitic capacitance

K_{VCO} fluctuation degrades the performance of the PLL, so it must be suppressed when the wide frequency range is necessary. Moreover, a current of a charge pump must be changed with K_{VCO} to attain a constant PLL loop gain for stable operation [5].



(a) ideal (b) conventional

Figure 3. VCO tuning characteristics

4. Reducing K_{VCO} Fluctuation Technique

To suppress K_{VCO} fluctuation for wide-band VCO design, we introduce the self-controlled varactor block configuration as shown in Figure 4. The unit cell consists of two serially connected varactor (C_v) and biasing capacitor (C_b), and additional two switches to control the varactor capacitance tuning. There are four self-controlled varactor blocks, and each block has three unit cells. V_{DD}, $V_{DD}/2$ and 0 V are biased to each varactor block for linear frequency tuning feature [6]. A schematic diagram of the VCO with the proposed technique is depicted in Figure 5.

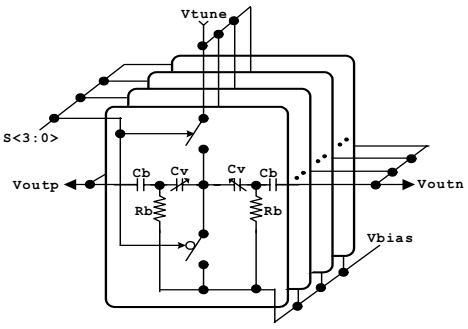


Figure 4. Self-controlled varactor configuration

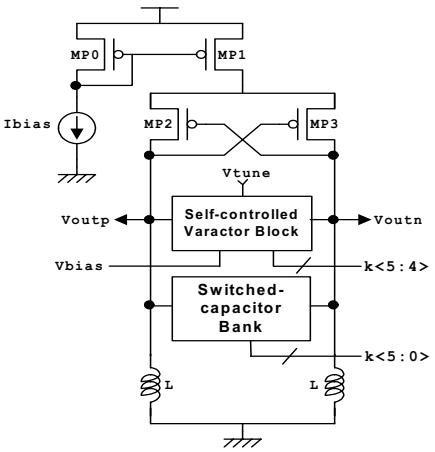


Figure 5. Proposed small K_{vco} fluctuation VCO

The upper 2-bit k<5:4> of 6-bit switched-capacitor bank code k<5:0> is used to control the frequency-voltage gain characteristics, which can make linearly controlled four different VCO-gain curves as shown in Figure 6. Therefore, because K_{VCO} is larger for the higher frequency band and smaller for the lower frequency band, by selecting the larger K_{VCO} curve for the lower frequency band and the smaller K_{VCO} curve for the higher frequency band, we can reduce K_{VCO} variation.

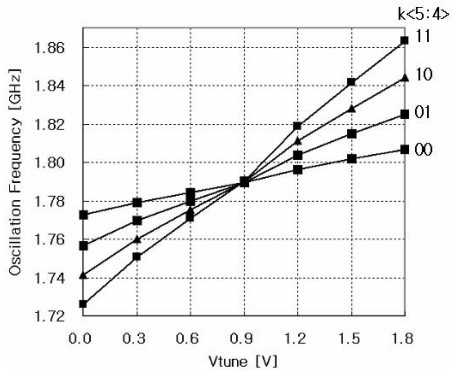
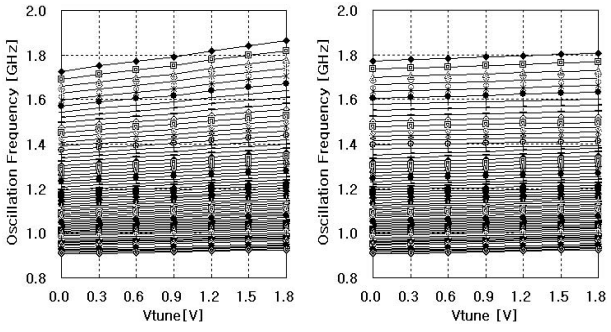


Figure 6. Self-controlled VCO-gain characteristics

In this work, a conventional 6-bit capacitor-bank type VCO is compared for the feasibility check of the proposed K_{vco} suppression technique, and the target frequency band of VCO is specified as the range from 890 MHz to 1.8 GHz which meets the requirements of the DVB-H/ISDB-T/T-DMB receiver. Figure 7 shows the simulated frequency-voltage gain curves of the conventional and proposed VCOs. Each VCO exhibited 64 frequency curves by setting k<5:0> to control the total capacitance of the switched-capacitor banks. As illustrated in Figure 8 and Table 2, the conventional VCO exhibited maximum K_{vco} of 76.3 MHz/V and minimum K_{vco} of 10.2 MHz/V, so K_{vco} Variation is ±76.4%. The proposed VCO exhibited maximum K_{vco} of 19.0 MHz/V and minimum K_{vco} of 8.8 MHz/V, so K_{vco} variation is ±36.7%, which is suppressed to about half of the conventional VCO.



(a) conventional (b) proposed

Figure 7. Frequency vs. control voltage of the VCO

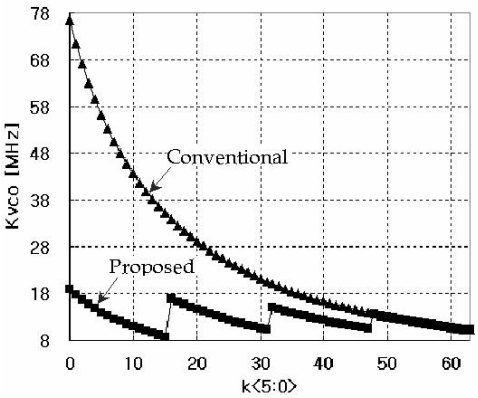


Figure 8. VCO-gain (K_{vco}) characteristics

Table 2. Summary of K_{vco} characteristics

	Conventional	Proposed
K_{vco} Max.	76.3 MHz/V	19.0 MHz/V
K_{vco} Min.	10.2 MHz/V	8.8 MHz/V
K_{vco} Variation	±76.4%	±36.7%

5. Fractional-N Frequency Synthesizer Design

There are many kinds of Σ-Δ modulator (SDM) schemes, and the authors used the 3rd-order reconfigurable sigma-delta modulator for phase noise shaping, and a 1-bit quantizer architecture for simple and stable operation [7]. The 3rd-order single stage SDM consists of three accumulators and six coefficients. The noise transfer function (NTF) of SDM is obtained as equation (2) and the design was verified with MATLAB Simulink and ModelSim co-simulation method. Figure 9 shows the phase noise characteristics of the designed fractional-N synthesizer against offset frequency from the oscillation frequency.

$$H_{NTF}(z) = \frac{z^3 - 3z^2 + 3z - 1}{z^3 - 1.162z^2 + 0.6959z - 0.1378} \quad (2)$$

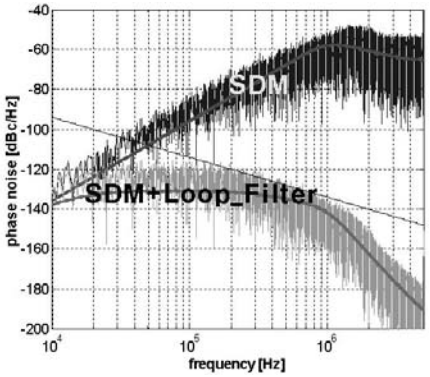
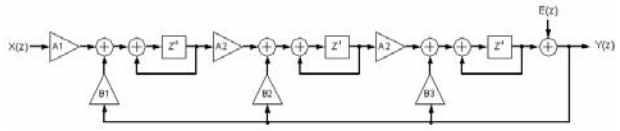
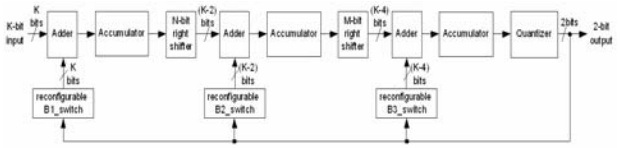


Figure 9. Phase noise characteristics

After the SDM designed with MATLAB Simulink satisfies the phase noise specification, it is implemented by logic blocks that consists of adder, accumulator, switch, and so on for ModelSim block diagram as shown in Figure 10(b). The design of digital logic block is possible with Verilog and simulated by HDL code in ModelSim. The SDM that consists of Verilog code generates digital waveform in result. But, the result of the ModelSim simulation is difficult to check the desired frequency characteristics. But the ModelSim-Simulink co-simulation using ModelSim simulation results could confirm the desired SDM frequency characteristics.



(a) MATLAB Simulink implementation



(b) ModelSim implementation

Figure 10. The relation of SDM block diagrams

Figure 11 shows a layout of the proposed FNFS, which occupies the area of 2720μm×2090μm. The VCO layout is arranged as symmetrically as possible and all capacitors and transistors are placed nearby, so energy loss due to connection wires can be reduced.

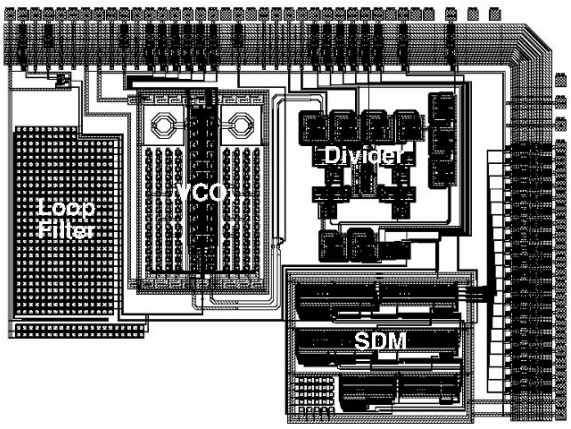


Figure 11. Layout of the designed FNFS

6. Conclusion

In this paper, a fully integrated wide-band FNFS with a reducing K_{VCO} fluctuation technique is presented. The designed FNFS consumes 11.4 mA from a single 1.8-V supply voltage and the experimental results show -80 dBc/Hz in-band phase noise and -127 dBc/Hz out-of-band phase noise at 1 MHz-offset frequency. The tuning range is as wide as 890 MHz (52%) from 910 MHz to 1.8 GHz, which can cover all the desired frequencies for the DVB-H/ISDB-T/T-DMB receivers. By adding four self-controlled varactor blocks to conventional 6-bit switched-capacitor bank LC VCO configuration, we achieve 52% smaller K_{VCO} fluctuation than that of a conventional design. The proposed FNFS has the suppressed VCO-gain fluctuation while maintaining a wide tuning range and without additional bias current at low cost, so it is well suited for multi-band and multi-mode mobile applications.

Acknowledgment

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