A Study on Fast Locking and Wideband PLL

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Abstract

In this paper , a dual-slope phase frequency detector and charge pump architecture for fast locking of PLL is proposed and analyzed. The proposed PLL circuit is designed based on the 0.11um CMOS process with 1.2V supply voltage. The modified delay cell circuit of Ring Oscillator is used in the design of VCO and the frequency range of VCO is from 23MHz to 522MHz. This frequency synthesizer has a good linearity characteristic.

1. Introduction

The CMOS frequency synthesizers and the phase-locked loops have been widely used in many modern wireless communication systems. Low phase noise, fast locking, and wide frequency tuning range are essential requirements for mobile electronic systems. In order to meet wide frequency range and to achieve the fast locking, the frequency tuning range of 23MHz ~ 522MHz of PLL with a dual-slope phase frequency detector was designed in this paper. There are three parts in this paper. The first part introduces the circuit design of PLL. The second part shows the design of PFD and VCO circuits, and last part is simulation result and summary.

2. PLL Design

The basic structure of frequency synthesizer is shown in Fig.1. Among them, VCO is the core of frequency synthesizer. The most frequently used VCO's fabricated in CMOS process is LC oscillators and ring oscillators. Although LC oscillators have advantages in phase noise suppression, it also have many disadvantages, such as large area, the difficulty of designing inductor with high Q value in present CMOS process, and narrow tuning range etc. On the contrary, CMOS ring oscillators have been used widely since it has small area, wide tuning rang, good linearity, and require no external device while it could be easily designed and fabricated in CMOS process. Among CMOS ring oscillators, the differential ring oscillators are generally adopted in applications for precise frequency control.

3. PFD and CP Design

The proposed PFD topology is based on two loops, the fine-tuning loop and a coarse-tuning loop as shown in Fig.2. For fast frequency lock, a coarse-tuning loop is used to accelerate the lock time and fine-tuning loop is used to complete fine adjustments. When the phase difference Φe of two input signals ref and feedback is smaller than Φd, the fine-tuning loop operates and fine CP circuit will produce current. On the other hand, if phase difference Φe of two input signals is larger than Φd, then two loops operate at the same time, and then, the operation is continuous until the phase difference Φe is reduced to Φd, so the locking time is reduced by coarse-tuning loop. If the Φe is smaller than Φd, the coarse-tuning loop stops working. The fine PFD circuit design adopts the conventional PFD structure which consists of 2 DFF circuit and a NOR gate. The design of coarse PFD circuit is shown in Fig.3. Conventional static CMOS circuit is used in the coarse PFD. The dead zone of coarse PFD is larger than the fine PFD, but not so large enough to turn off coarse-tuning operation. Since the CP output current Ic is controlled by the coarse PFD output signal up1 and dn1, these two signals need to be turned off when the phase difference Φe is smaller than Φd. If the turn-off range is not wide enough, the VCO control voltage Vc will be perturbed by the large current Ic and the jitter performance of the PLL will be degraded. The dead zone width of coarse PFD is controlled according to the adjustable pulse width scheme(APW) which can stop the coarse PFD operation with the one-short signal that is produced by APW. The turn off range of the APW is controlled by Vc which is the control voltage of VCO. So the dead zone of the coarse PFD is automatically tuned according to the control voltage Vc.[1]

4. VCO Design

About the design of the VCO, this paper uses the differential Ring Oscillator mode. The structure of VCO is shown in Fig.4. The proposed VCO includes bias and buffer circuits. We adopted the symmetric load construction into the delay cell circuit of Ring Oscillator. Compared with triode mode, the symmetric mode have good linear characteristic and strong resistance interference ability for external influence. The proposed VCO includes bias and buffer circuits. Conventional symmetric circuit's frequency range is very narrow. To achieve wide tuning-range, we used a new delay cell. The schematic of new delay cell is shown in Fig.5. It includes two modified symmetric loads, positive partial feedback and two added cascade mode PMOS. The positive partial feedback which is generated by transistors MN2 and MN3 provide the required bias condition for the circuit to oscillate。 Meanwhile, 2 cascade mode are added to the delay cell of VCO to increase the operating frequency range.[2]。 The bias circuit is shown in Fig.6. This circuit generates the voltage V_{bias} which is the gate voltage of symmetric load. V_{bias} controls the resistance of the load. The circuit uses positive feedback structure, providing transistor P_4 with the variable gate voltage which enables V_{bias} to track with the change of V_{ctrl} quickly. The bias circuit adopts the self-cascode structure which could offer the proper and stable bias voltage。 PMOS4 is to ensure that Vbias does not generate drift phenomena when PMOS3 is closed and has almost zero current。

5. The simulation result

We use 0.11um CMOS process with 1.2V supply voltage to design the proposed frequency synthesizer. Cadence Spectre tool is used for the circuit simulation of frequency synthesizer.

The simulation of VCO output in shown in Fig.7. From the result, the tuning range of VCO is from 22.8MHz to 522MHz.

Fig.8 is the locking result of PLL with the lock detector circuit and conventional PLL. From the result shown here, compared with the conventional PLL, the PLL with lock detector circuit shows fast locking performance.

6. Summary

The fast locking PLL using 0.11um CMOS process with 1.2V supply voltage is proposed and the coarse PFD and the modified delay cell are used in this paper. The output frequency range of VCO is from 23MHz to 522MHz, according to the simulation results, the coarse PFD accelerate frequency lock compared with

conventional PFD circuit. Modified delay cell circuit shows good linear characteristic. The whole circuit is designed using Cadence Spectre tool and verified by it.

References

[1] Kuo-Hsing Cheng; Wei-Bin Yang; Shu-Chang Kuo, "A dual-slope phase frequency detector and charge pump architecture to achieve fast locking of phased-locked loop" Circuits and Systems, 2004. ISCAS, Page(s): I-777-80 Vol.1, 2004

[2] Tuan-Vu Cao; Wisland,D.T Lande,T.s; Moradi,F, "Low-Voltage, Low-power, and wide-Tuning-Range Ring-VCO for Frequency ΔΣ Modulator," NORCHIP, pp.79-84,2008.

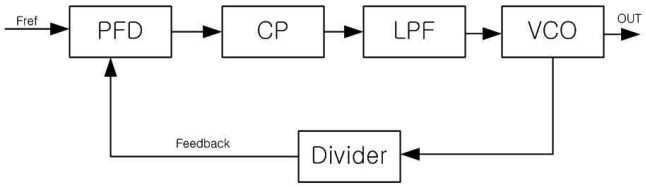

Fig.1 PLL Structure

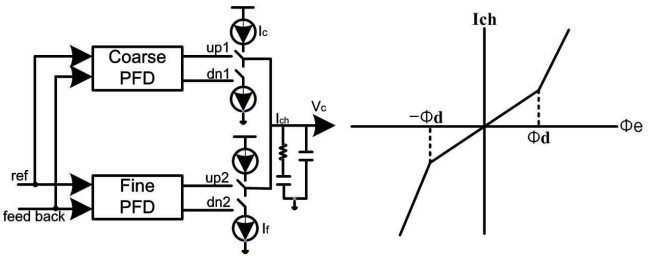

Fig.2. The two Loop Scheme of PFD

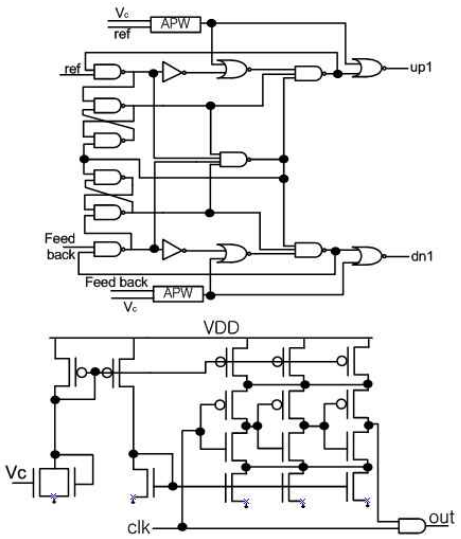

Fig.3. The coarse PFD and APW circuit

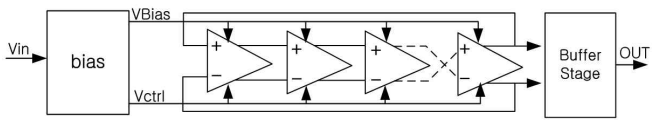

Fig.4. VCO Structure

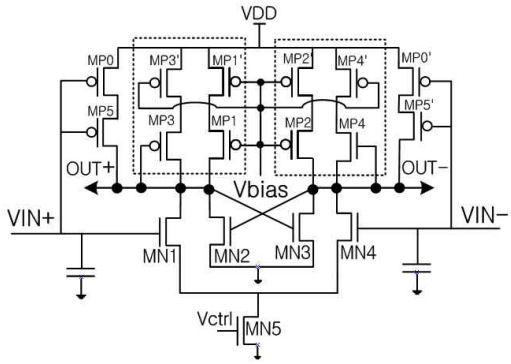

Fig.5. Delay Cell Circuit

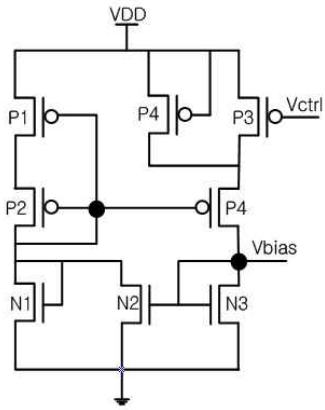

Fig.6. Bias Circuit

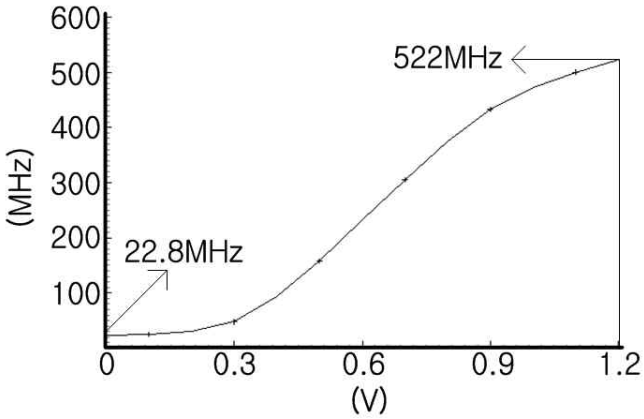

Fig.7. The output of VCO

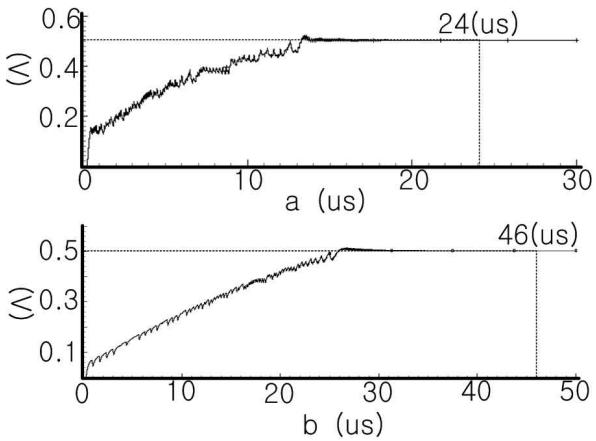

Fig.8. (a) PLL with lock detector (b) conventional