A Study of PLL with Power Down Mode and Lock Detection

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Abstract

This paper introduces general purpose PLL with power down mode and lock detection circuit. 0.11μm CMOS process with 1.2V supply voltage is used for design. The VCO frequency range is from 23MHz to 522MHz. The PLL locking status could be known by lock detection circuit and the PLL can be locked quickly when system is turned on from the power down mode to wake up mode. The relocking time is less than 1μs from the simulation of total PLL.

Keywords : PLL Lock Detection Power Down

Ⅰ. Introduction

Along with the development of the communication technology, there are a lot of electronic products has been developed and widely used. Among them, the CMOS frequency synthesizers and the phase-locked loops(PLL) have been widely used in many modern wireless communication systems. Conventionally, the PLL is an analog circuit where the locking information is stored as an analog signal. Holding the analog locking information is very difficult, because the information can be lost when the PLL system is turned off during the power down state. Therefore, the power consumption will increased in power down states due to PLL. In order to solve this problem, this paper implement a circuit which holds the locking information during the power down state. The proposed circuit is made of an ADC circuit and a DAC circuit. The detailed description of power down operation and the simulation results are given in the following sections.

Ⅱ. The Structure of PLL

As conventional PLL, the proposed structure includes VCO, frequency divider, phase frequency detector(PFD), charge pump(CP), and loop filter. The difference from the conventional PLL is power down mode and lock detection which store the locking information and detect the locking of the PLL. The proposed PLL is shown in Fig. 1.

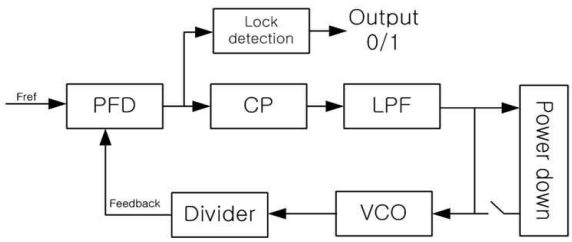

Fig. 1 Proposed PLL structure

1.VCO Design

In this paper, the VCO uses the ring oscillator architecture of which frequency tuning range is from 23MHz to 522MHz. We use the differential ring oscillator type in this work. The structure of VCO is shown in Fig. 2. The VCO includes bias and buffer circuits.[1]

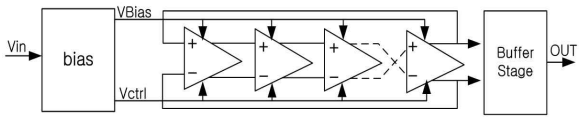

Fig. 2 VCO Structure

2.Lock Detection Circuit

The lock detection circuit is shown in Fig. 3. Conventional lock detection circuit has analog and digital structures. In this paper we adopted analog structure. As shown in Fig. 3, the circuit contains a XOR gate and a comparator circuit. The XOR gate generates a pulse signal which is the phase error of two input signals, which are phase error between reference signal and VCO signal. This pulse signal will be integrated and compared with 0.5*VDD by comparator, and then, the comparator outputs "high" or "low". "High" means the PLL is locked and "low" shows the PLL has not reached locking state.[2]

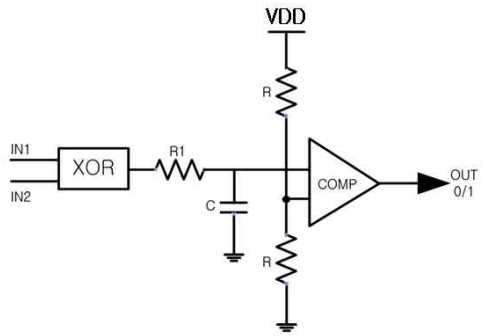

Fig. 3 Lock Detection Circuit

Comparator is often placed in a very noisy environment in which it must detect signal transitions at the threshold point. If the comparator is fast enough and the amplitude of the noise is great too, so the output will not be correct. In order to solve the above problem, we adopted a two stages hysteresis amplifier in the design of comparator which is shown in Fig.4.

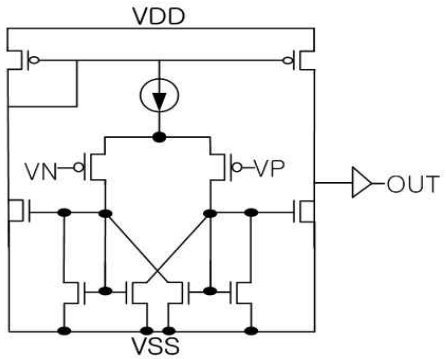

Fig. 4 Hysteresis comparator circuit

3. Power Down Circuit

The proposed power down circuit is shown in Fig. 5. The circuit includes an ADC and a DAC which forms a loop that can store the locking information and supplies the information to VCO when the system wakes up again. The 6bit ADC and 6bit DAC are used in this paper. The schematic is shown in Fig. 6. The design of 6bit DAC use a charge scaling DAC which has a good accuracy and fast operating speed. 6bit ADC design is shown in Fig.6. The circuit includes a comparator and a 6bit up-down counter which generate signals with the comparison result of two input signals. When the PLL has entered into locking states, the ADC-DAC loop goes in locking states too. The locking information is stored in digital memory during the PLL is turned off and the system enter sleep mode. When the PLL system wakes up again, the data of locking will be supplied to VCO. So that, the time to lock PLL again will be reduced and the power consumption is decreasing.[3]

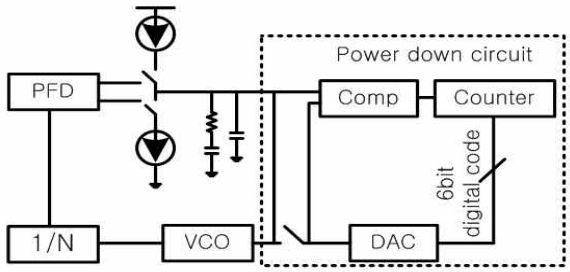

Fig. 5 Proposed PLL with Power Down circuit

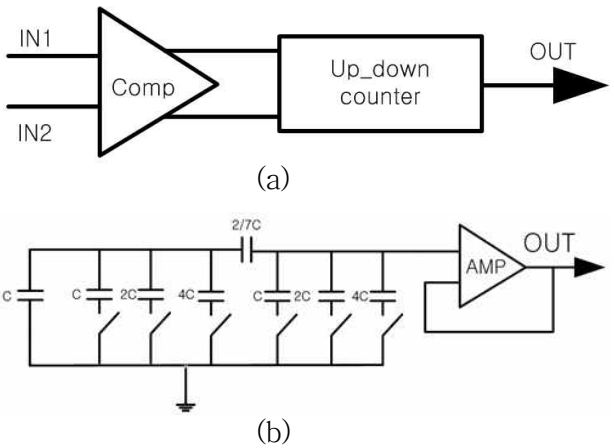

Fig. 6 (a) 6bit ADC and (b) 6bit DAC circuit

In order to increase output characteristics of DAC, the cascode amplifier is used as a unit gain buffer in the design of DAC. The schematic is shown in Fig. 7.

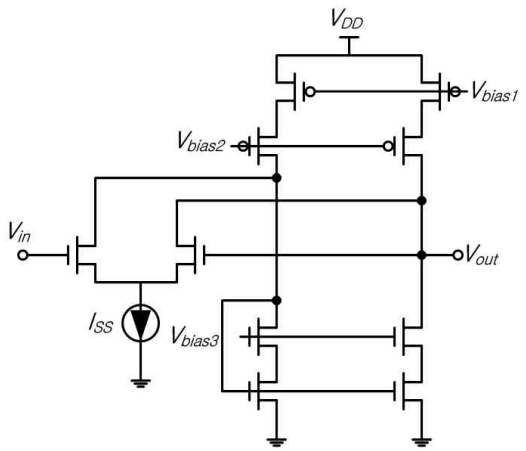

Fig. 7 Cascode amplifier

III. Simulation Result

The DAC simulation result is shown in Fig. 8. According to the simulation, the circuit have good accuracy and monotonicity.

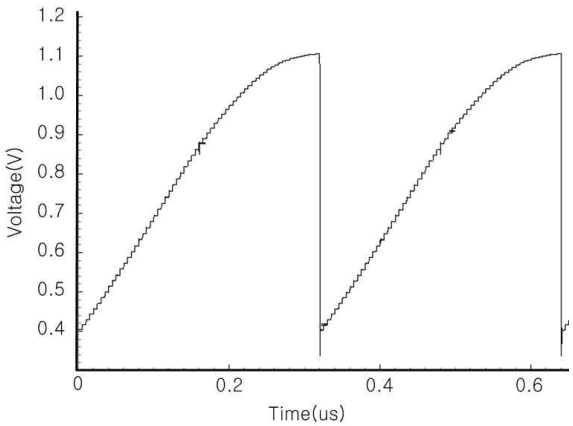

Fig. 8 DAC simulation result

Fig. 9 shows the output of ADC-DAC loop. Simulation result shows, when the output voltage of loop has reached reference voltage, then the output will be increased until the output reached the voltage of reference, and then the loop enter into locking states.

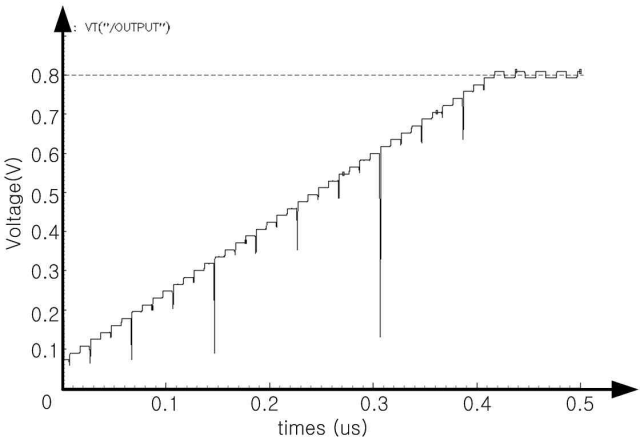

Fig. 9 The output of ADC-DAC loop

Fig. 10 shows the locking states of the proposed PLL(A) compared with the conventional PLL(B). According to the simulation result, the proposed PLL has a 1μs' improvement compared with the conventional PLL in the operation of turning on from sleep mode to locking state again. From the output of lock detection circuit, we can know PLL status and determine the locking time of PLL.

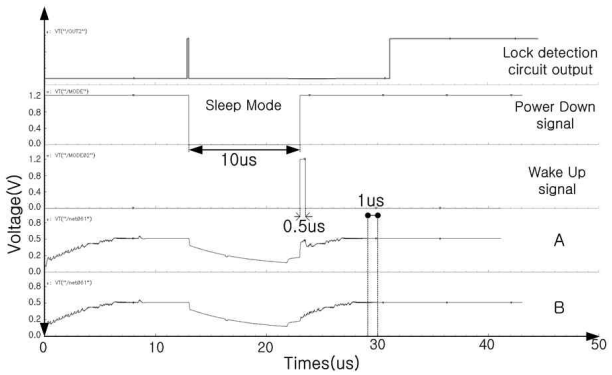

Fig. 10 The locking states of the proposed PLL(A) and the conventional PLL(B).

IV. Conclusions

The fast locking PLL with power down mode and lock detection circuit using 0.11μm CMOS process with 1.2V supply voltage is proposed in this paper. The output frequency range of VCO is from 23MHz to 522MHz, and according to the simulation results, the locking information can be stored in loop during the off state of PLL, thus,

the power consumption could be decreased. From the simulation result of lock detection circuit, we could know locking status and locking time. The proposed PLL could be used at the systems which have normal operation and power down mode.

References

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