The Design of Simple Lock Detection Circuits for PLL Application

Jun-Cheng Yong-Moon
Department of Electronic Engineering
Soongsil University
e-mail: chengjungood@nate.com, moony@ssu.ac.kr

Abstract

This paper introduced a PLL with the simple lock detection circuit. The simple digital lock detection circuit based on the A/D conversion of loop filter output is used in this paper. So the locking of PLL could be determined accurately by the proposed lock detection circuit.

I. Introduction

CMOS frequency synthesizers and phase locked loop(PLL) have been widely used in many modern wireless communication systems. Currently, we determine the locking status of PLL by detecting the states of control voltage of VCO, but the locking detection for PLL using previous method is not accurate and detection circuit is complex, so we designed a simple digital lock detection circuit for solving this problem in this paper. The proposed circuit and its operation will be described in detail in following sections.

II. The Design of PLL

2.1 The Structure of PLL

Compared with conventional PLL, the proposed PLL includes basic PLL blocks and digital based lock detection circuit. The lock detection circuit determines the locking status of PLL which is important in system level. The proposed structure of PLL is shown in Fig. 1.

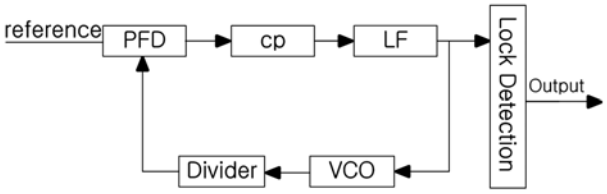

Fig. 1 Proposed PLL structure

2.2 Lock Detection Circuit

The block diagram and the proposed lock detection circuit are shown in Fig. 2 and Fig. 3, respectively.

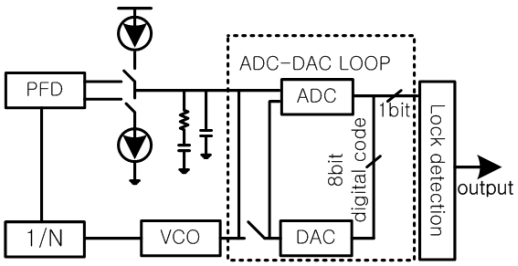

Fig. 2 Block diagram of lock detection

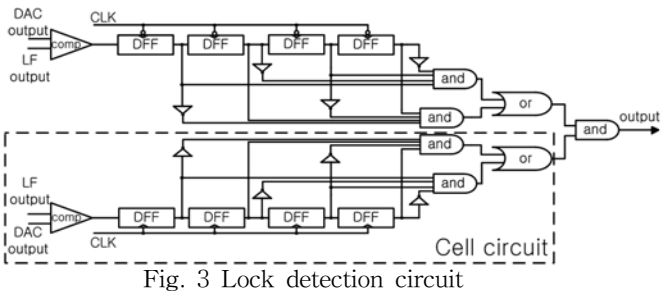

Fig. 3 Lock detection circuit

Fig. 2 shows the structure of lock detection circuit which is based on the ADC-DAC loop which is used for converting the analog information into the digital information.[1] When the PLL system has achieved locked status, the ADC-DAC loop will goes into stable condition, and at the same time, the output of the comparator of the ADC will produces alternating Up and Down pulse signals. So we can could use the lock detection circuit as shown in Fig. 3 to determine the status of PLL. According to the Fig. 3, the loop filter output is compared with the DAC output by the comparator of the ADC which outputs 1 bit digital information that will pass the cell circuit. The cell circuit consists of 4 DFFs, 4 inverters, 1 OR gate and 2 AND gates. When the output of the cell circuit is “High”, which means the PLL has reached locked status. On the contrary, when the output of cell circuit is “Low”, which means the PLL has not reached locked state. As Fig. 3 shows, the lock detection circuit has two cell circuits, the reason for this is to get more accurate results for locking status. Two cell circuit is almost similar except one thing. One of them uses negative edge-triggered DFF circuit, and the other adopts positive edge-triggered DFF circuit. So the result of detection for locking status using two circuits is more accurate. The 7-bit DAC and ADC circuits are used in this paper. The design of 7-bit DAC uses the charge scaling DAC which has good accuracy and fast operating speed. The schematic of 7-bit DAC circuit is shown in Fig. 4. 7 bit ADC design is shown in Fig. 5. The circuit includes a comparator and a 7 bit up-down counter which generates signals with the comparison result of two input signals. When the PLL has entered locked states, the ADC-DAC loop goes into locked states, too.[2][3]

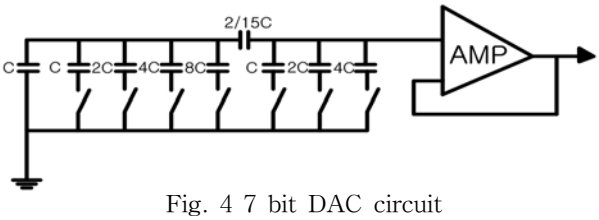

Fig. 4 7 bit DAC circuit

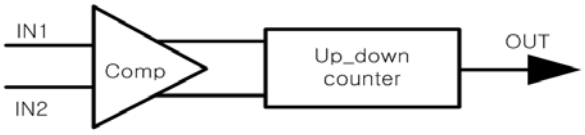

Fig. 5 7 bit ADC circuit

Ⅲ. Simulation Result

Fig. 6 shows the simulation result of 7-bit DAC, according to the simulation, the circuit have good accuracy and monotonicity.

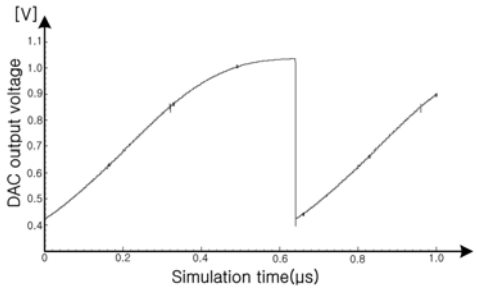

Fig. 6 DAC simulation result

Fig. 7 shows the output of ADC-DAC loop. Simulation result shows that the output voltage of loop has reached constant voltage. The output will be increased until the output reaches the reference voltage for the locking voltage of reference, and then the loop enter locked state.

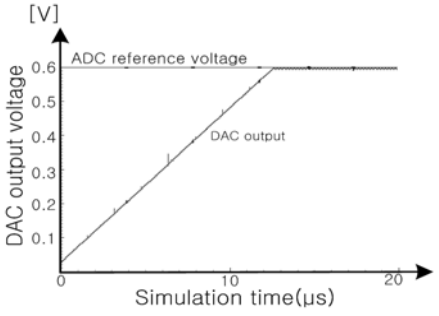

Fig. 7 The output of ADC-DAC loop

The locked state of PLL is shown in Fig. 8. According to Fig. 8, when the PLL enters locked state, the output of lock detection is “High”, and before entering locked state, the output is “Low.”

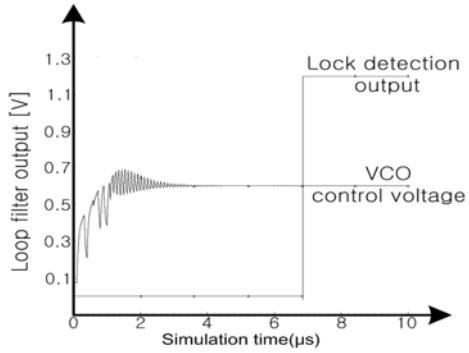

Fig. 8 The locked state of PLL

Ⅳ. Conclusions

The PLL with a simple lock detection circuit using $0.11\mu m$ CMOS process with 1.2V supply voltage is proposed in this paper. According to the simulation result of lock detection circuit, we could easily determine the locking status of PLL. The proposed PLL could be used in foundry for IP support due to its function and accurate locking detection.

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