Design of CMOS LC VCO and Prescaler for Tri-band WLAN Applications

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Abstract

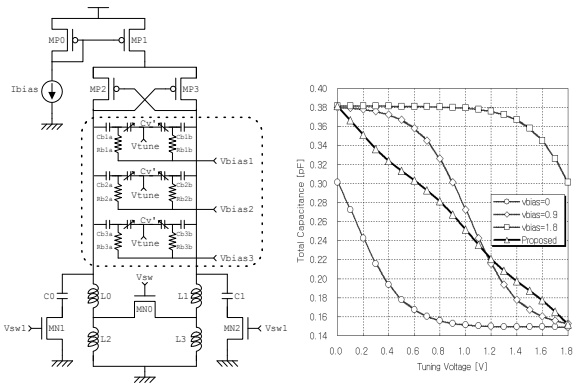
CMOS LC VCO and quadruple modulus prescaler for tri-band wireless LAN applications were designed using 0.18㎛ CMOS process. The VCO operation was verified for 5.8GHz band (5.725~5.825GHz), 5.2GHz band (5.150~5.325GHz), and 2.4GHz band (2.412~2.484GHz) using the switchable LC resonators. To linearize its frequency-voltage gain, the optimized multiple MOS varactor biasing technique was used. The 16/17/20/21 quadruple modulus prescaler utilizes the differential SCL structure for switching noise reduction and stable operation upto 3GHz.

1. Introduction

Specification of recent wireless communication employs three standards of IEEE 801.11a, 801.11b, and 801.11g.[1] According to market's need, a system to support more than three specifications with its low cost is needed. Key block in frequency synthesizer to meet this need is VCO(Voltage Controlled Oscillator) and prescaler.[2] Supporting tri-band using three VCOs are possible, but a VCO to cover all tri-bands is more desirable.[3-4] Differential LC oscillator using spiral inductors and switched-capacitor bank is used in VCO. Proposed prescaler uses SCL(Source Coupled Logic) structure with differential signaling and is operated at very high frequency.[5]

2. VCO

Fig. 1.(a) shows the designed CMOS LC VCO with linearized VCO gain. PMOS transistors are chosen for VCO core to reduce flicker noise. In fig. 1.(a) the block with dotted line shows the capacitance linearization circuit using three varactor bias voltages, and fig. 2.(b) shows its C-V curve. With the bias voltage of 0V, the capacitance has a linear range in low voltage. It has a linear range in middle voltage with 0.9V bias voltage, and a linear range in high voltage with 1.8V bias voltage. Therefore, if three curves of different bias voltages (0V, 0.9V and 1.8V) are superposed, we can get the linearized C-V curve for the whole range.

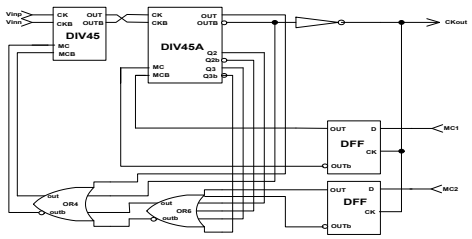


(a) (b)

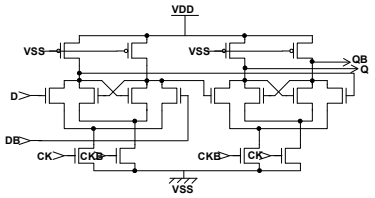
Fig. 1.(a) CMOS LC VCO with linearized gain
(b) C-V curve linearization

3. Prescaler

Fig. 2.(a) shows block diagram of quadruple modulus prescaler capable of four division ratios. Prescaler receives signals from 2.3GHz to 5.85GHz in frequency, but divide-by 2 block is used to lower frequency. So the frequency range of 4.9 to 5.85 is lowered to 2.3 to 2.925GHz. In case of 40MHz comparison frequency, division value of 58~73 is in need. So dual modulus prescaler can not cover all channels. To enhance this, use of quadruple modulus with four division value brings to synthesize all desired channels. The division ratio(16/17/20/21) of prescaler is decided by control signals(MC1, MC2) and both V_{inp} and V_{inn} are inputs receiving differential output of VCO. First division component (DIV45) which receives VCO inputs consists of three D flip-flops and needs stable high speed operation and low noise characteristic due to running at high frequency upto 3GHz. Fig. 2.(b) represents D flip-flop used in the design of prescaler with differential SCL structure in order to reduce noise from substrate and power lines for stable running in high operation frequency.[6]



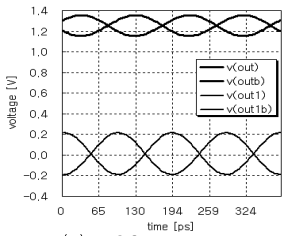
(a)



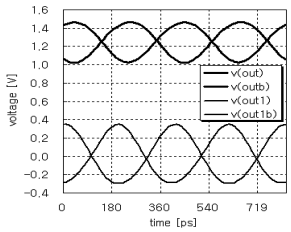
(b)

Fig. 2.(a) Quadruple modulus prescaler
(b) SCL type D F/F

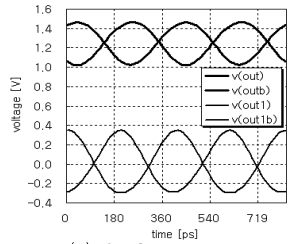
4. Simulation Results and Layout



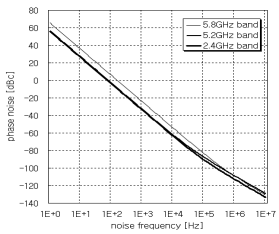
(a) 5.8GHz band



(b) 5.2GHz band



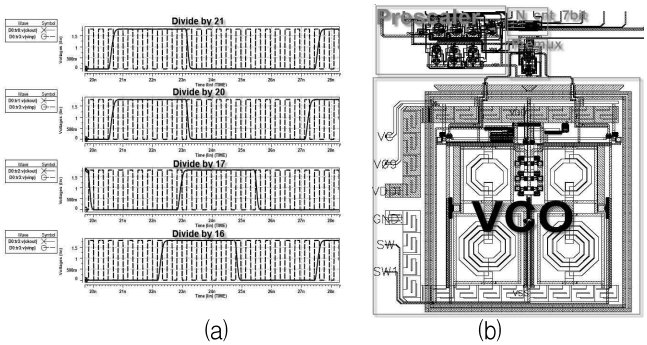
(c) 2.4GHz band



(d) VCO phase noise characteristic

Fig. 3. VCO output level and phase noise characteristic

Comparative simulation for VCO and prescaler is carried out by ADS and Hspice. Post layout simulation including layout parasitics is also carried out in each case. Fig. 3 shows graphs of VCO output signal waveforms and phase noise characteristics. Fig. 3.(a)~(c) show each VCO output of 5.8, 5.2 and 2.4GHz band. Fig.3. (d) is a plot of phase noise characteristics based on 1/f noise of VCO and shows that noise level of −110dBc/Hz at 1MHz offset is possible. Fig. 4.(a) is a graph representing prescaler division operation depending on control signals. From the top, it shows division of 21/20/17/16 in order. Fig. 4.(b) is the layout of VCO and prescaler and symmetric layout is performed for differential signal characteristics. Finger−type transistors are used for high frequency operation to minimize RC parasitics.



(a) (b)

Fig. 4.(a) Quadruple modulus prescaler simulation (division of 21/20/17/16)
(b) Layout of the designed VCO and prescaler

5. Conclusion

A tri−band(5.8GHz, 5.2GHz, 2.4GHz) CMOS LC VCO with linearized gain and a 21/20/17/16 quadruple prescaler for WLAN applications were designed using 0.18um CMOS process. VCO phase noise at 1−MHz offset was less than −110dBc/Hz for all band. The prescaler adopted SCL sturcture to reduce the switching noise, and had a maximum operation frequency of 3GHz. The designed VCO and prescaler dissipate 12.6mW, and occupy 570μm×1130μm die area.

References

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