Available online at www.sciencedirect.com
SCIENCE DIRECT®
Current Applied Physics 5 (2005) 237–243
Current Applied Physics
Physics, Chemistry and Materials Science
www.elsevier.com/locate/cap

Design and analysis of low power memory using efficient charge recovery logic circuits ☆

Chanho Lee *, Inho Na, Yong Moon

School of Electronic Engineering, Soongsil University, Sangdo-5-dong, Dongjak-ku, Seoul 156-743, South Korea

Received 13 August 2003; accepted 23 September 2003
Available online 17 June 2004

Abstract

ECRL (efficient charge recovery logic) circuits can reduce the energy consumption compared with that of the static circuits. The ECRL circuits have been applied to the combination logic. However, storage elements are also required for most of digital circuits. A simple structure of an ECRL latch is proposed for a storage element. It consists of an ECRL inverter, an ECRL NAND gate, and two MOSFET switches, and it has input signals of 'enable', 'input', and 'reset'. A 16×8-bit shift register file is designed using the latches and a specially designed power supply which generates 4-phase oscillatory waves. The efficiency of the energy consumption is improved by about 50% as the changing rates of the input values are decreased, and it is not affected by the power supply clock frequency in the range of 100–400 MHz. The energy consumption of the proposed circuit is about half of that of the static CMOS TSPCL (true single-phase clocked logic) register.

PACS: 85.40.Bh
Keywords: Adiabatic circuit; Low energy memory; ECRL

1. Introduction

The power consumption of electronic devices increases rapidly as the operating time and the performance of the electronic devices increase with the change of our lifestyle. Moreover, the mobile devices require high performance, light weight, and long operation time, which are contradictory [1–3]. One of the possible solutions is to reduce the energy consumption of the circuits while keeping the same performance. The energy consumption of adiabatic circuits is greatly reduced by returning charges to power supplies after the circuit operation [3–9]. The energy loss of adiabatic circuits consists of adiabatic energy loss, non-adiabatic energy loss, and the basic energy loss due to the leakage current of MOSFETs. The adiabatic energy loss and the energy loss due to the leakage current are not avoidable. The adiabatic energy loss is proportional to the product of load capacitance and on-resistance of a MOSFET when we regard the MOSFET as a switch, and it is inversely proportional to the slope of the power supply waveform. The energy loss due to the leakage current is caused by the leakage current which is independent of the power supply slew rate. The non-adiabatic energy loss is caused by the threshold voltage which is needed to turn on the MOSFET switch. The RERL (reversible energy recovery logic) is proposed to reduce the non-adiabatic energy loss [7]. Though the non-adiabatic energy loss is minimized using the RERL, the large number of additional circuits for reversible computing degrades the energy efficiency at high frequency operation. The RERL shows good energy consumption characteristics below 2 MHz operation compared to the conventional CMOS logic [7]. This kind of logic is suitable for the application where the operation frequency is not important and the energy consumption is of concern. In this paper, ECRL (efficient charge recovery logic) is used because the energy consumption is lower than the conventional CMOS

☆ Original version presented at the 10th Korean Conference on Semiconductors, Seoul, Korea, 27–28 February 2003.

* Corresponding author. Tel.: +82-2-820-0710; fax: +82-2-821-7653.
E-mail address: chanho@e.ssu.ac.kr (C. Lee).

1567-1739/$ - see front matter © 2004 Published by Elsevier B.V.
doi:10.1016/j.cap.2003.09.021

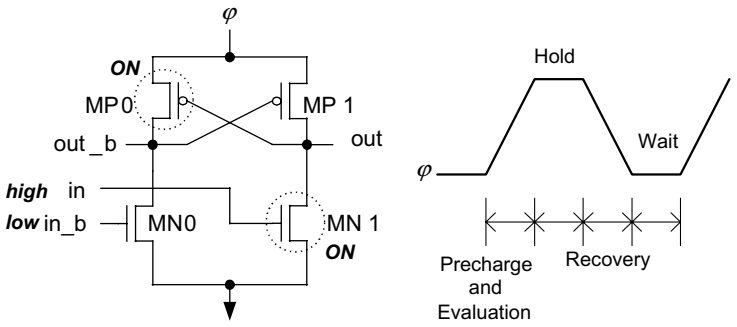

Fig. 1. The basic structure of an ECRL inverter and operation phases of supply clocks.

logic in high frequency operation though the non-adiabatic loss exists [8,9].

The ECRL circuits use a differential signal scheme so that an inverter can also be used as a buffer, and the supply clocks are divided into 4 operation phases. Fig. 1 shows a basic ECRL inverter. The 'in_b' and 'out_b' signals are the complementary signals of 'in' and 'out' signal, respectively. (From now on, the signal name with the suffix '_b' means the complementary signal.)

The 1st phase of ECRL circuit is 'precharge and evaluation' in which the input values are sampled and the output nodes are charged or discharged depending on the inputs. The stored input values are held in the 'Hold' phase for the next stage, and the stored charge is recovered during the 'Recovery' phase. The input signal can be changed during the 'Wait' phase. In Fig. 1, 'in' is '1' and 'in_b' is '0' initially, and so the MN0 is 'off' and MN1 is 'on' state. If the MN1 is 'on,' the node charge of 'out' is discharged to GND and MP0 is turned on by the value of 'out' node. In the 'precharge and evaluation' phase, 'out_b' node is charged to '1' through MP0 and 'out' node goes to '0' by MN1. The 'out' and 'out_b' nodes hold the values during the 'Hold' phase so that the next stage can update its values in the 'precharge and evaluation' phase. The supply clock goes down in the 'Recovery' phase, and the charge of 'out_b' node is returned to the supply clock, which carries out the recovery of the supplied energy. Fig. 2 shows the waveform of the energy recovery when the inverters are connected in cascade.

It has been reported that the energy consumption of the combinational logic circuits using the ECRL was reduced about 50% compared with the conventional CMOS circuits [8,9]. Although the memory elements to store data are necessary for a system, the ECRL memory element circuit is not announced yet. In this paper, a simple ECRL latch which is composed of one inverter, one NAND gate, and two MOSFET switches is proposed. The proposed latch has the input signals of 'enable', 'input' and 'reset'. The characteristics of the latch are analyzed, and the operation of a 16×8-bit shift register file with a power supply clock generator is also verified.

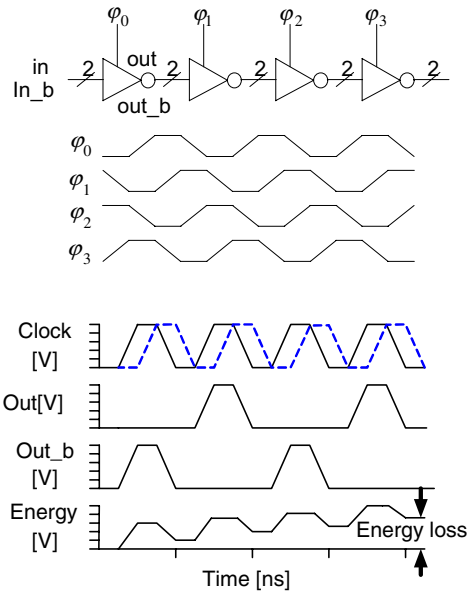

Fig. 2. The energy recovery of an ECRL inverter chain.

2. Design of ECRL latch

The ECRL circuits are operated in pipelining style with the 4-phase supply clocks. When the output is directly connected to the input of the next stage (which is a combinational logic), only one phase is enough for a logic value to propagate. However, when the output of a gate is fed back to the input, the supply clocks should be in phase. A latch is one of the simplest cases which have a feedback path. The input signals propagate to the next stage in a single phase, and the input values are stored in 4-phases (1-clock) safely. Fig. 3 shows the basic structure of the proposed latch. The thick lines mean two complementary signals. The forward NAND gate A1 can be replaced by a simple inverter when the reset function is not needed. When a DC input is applied, the differential sinusoidal waveforms can be obtained by propagating through an additional buffer. The signals from switching transistors, M1 and M2, drive the next stage through the NAND gate powered by φ_1. The

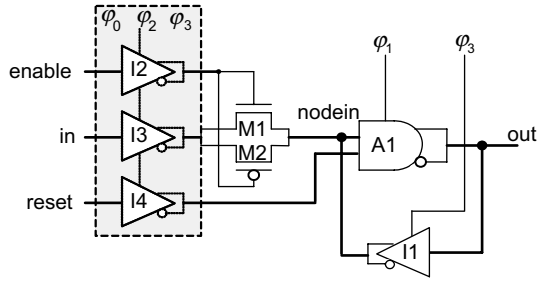

Fig. 3. The schematic of an ECRL latch.

buffer I1 for storing the signal is powered by φ_3, and the phase is in accordance with A1.

The buffer (I1) in the feedback path performs the 'precharge and evaluation' in the 'Recovery' phase of the NAND gate (A1) powered by φ_1. The waveform of the node 'nodein' changes abruptly near the beginning and the end of the waveform, and oscillates according to the phase of φ_3. Fig. 4 shows the waveform of the latch operation in which the input value is stored according to the 'enable' signal.

The gates driven by the output of the latch should be powered by φ_2, so that the 'precharge and evaluation' phase is accomplished during the 'Hold' phase of the latch. An input value applied to a latch propagates to the next stage in a single phase though 4-phases (1 clock) are necessary to store the input value to the latch safely because the input signal passes I1 and A1. The NAND gate A1 could be replaced by an inverter when the 'reset' function is not necessary.

Edge-triggered D flip-flops are commonly used in CMOS circuits because signals have glitches and the arrival times are not fixed. However, the signals of the ECRL circuits are synchronized to the supply clocks, and the arrival times of signals are almost the same so that the glitches are not produced. Therefore, the proposed simple latch is enough to perform storing operation correctly, and the gate count of the ECRL latch is very small compared with the conventional CMOS latch. In this paper, the TSPCL (true single phase clocked logic) flip-flop is selected for the energy comparison [10].

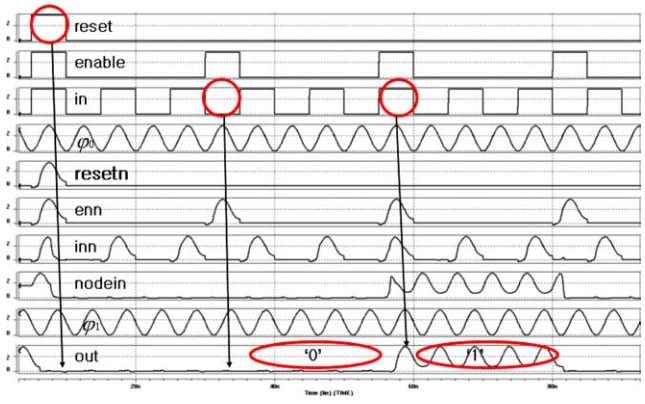

Fig. 4. The SPICE simulation result of the ECRL latch.

3. Characterization of the ECRL latch

The power supply clock applied to the buffer I2 in Fig. 3 can be any of φ_0, φ_2, φ_3. It does not change the logic operation of the latch though the energy consumption is affected. I2 feeds the 'enable' signal to control the switching transistors, and the control signal does not require the 'Hold' phase to transfer the signal to the next. If the phase of the power supply clock for I2 is φ_1, a phase confliction occurs at 'nodein' in Fig. 3, and the latch does not work properly. Supplying φ_1 to I2 can be avoided by appropriate buffering. The 'enable' signal of the ECRL latch plays the same role as the clock of the CMOS flip-flop which determines the sampling time of an input value.

The energy consumption of a latch depends on the flipping rate of the stored value and the 'enable' signal. The energy consumption of the latch shown in Fig. 3 is investigated by simulation when the flipping periods of input values are 10, 20, 40, and 80 ns, and when the 'enable' signal is always '1'. The results are shown in Fig. 5, and include the energy consumption of the buffers I2, I3, and I4. The period of the power supply clock is 10 ns (or the operation frequency of 100 MHz), and the phases of the power supply clock to the buffers I2, I3, and I4 in Fig. 3 are varied. The energy consumption decreases as the flipping period of the input values increase as expected. Fig. 5 shows that the phase of the power supply clock to the input buffers affects the energy consumption, and φ_2 gives the best result. The unreasonable energy consumption with φ_0 at the flipping period of 10 ns is due to the input buffers which are not parts of a latch. Table 1 shows the energy consumption

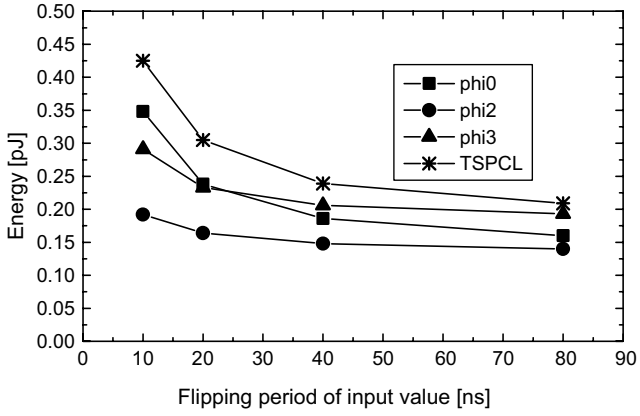

Fig. 5. The energy consumption of the ECRL latch and the CMOS TSPCL FF when 'enable' signal is always on.

Table 1
The energy consumption of each gate in the ECRL latch when 'enable' signal is always '1'

Energy consumption (pJ)	Phase of the power supply clock		
	φ_0	φ_2	φ_3
Total energy	0.348 (100%)	0.192 (100%)	0.291 (100%)
Input buffers I2, I3, I4	0.156 (44.8%)	0.005 (2.6%)	0.034 (11.7%)
NAND A1	0.007 (2.0%)	0.019 (9.9%)	0.018 (6.2%)
Switching MOS M1, M2	0.005 (1.4%)	0.003 (1.6%)	0.002 (0.7%)
Feedback buffer I1	0.180 (51.7%)	0.165 (85.9%)	0.237 (81.4%)

Always enable = '1'.
Flipping period of input values:10 ns.

of each gate. When the input buffers are powered by φ_0, the energy consumption of input buffers is about 45% of the total energy consumption. When φ_0 is applied to input buffers, the energy consumption at the input buffers is very large because the 'Recovery' phase of I1 is overlapped with the 'Hold' phase of input buffers, and the energy at 'nodein' is not recovered depending on the value of the node. When the flipping period of the input is large, the situation occurs much less frequently, and the energy consumption is comparable to the cases of the other power supply clock phases. In any cases, the energy consumption of the ECRL latch is much lower than that of the CMOS TSPCL.

Fig. 6 shows the energy consumption of the latch shown in Fig. 3 for the case that the 'enable' signal is '1' for 10 ns only when the input value changes. The MOS switch is on for 10 ns only when the 'enable' signal is '1', and the input signal does not reach the latch so that the latch does not change its value when the 'enable' signal is '0'. The energy consumption is smaller than that when the 'enable' signal is always '1' except for φ_2 case. When the input buffers are powered by φ_2, the MOSFET switches (M1, M2) are switched off in the 'Hold' phase, and the energy consumption in the MOSFET switches is high as shown in Table 2. Half of the energy is consumed by the switching transistors when the input buffers are powered by φ_2. The energy consumption of the input buffers is high when the input buffers are powered by φ_0. It is the same situation of the energy recovery problem as when the 'enable' signal is always '1' in Fig. 5.

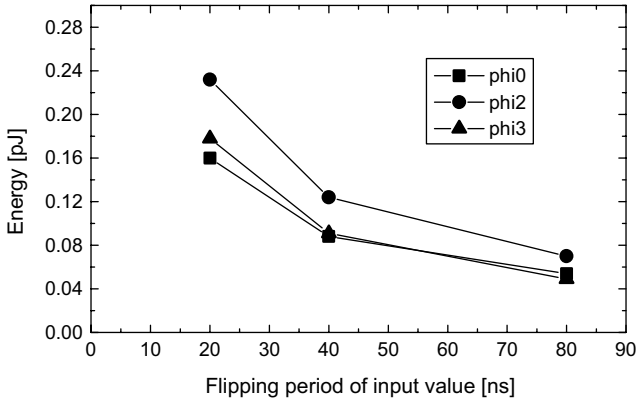

Fig. 6. The energy consumption of the ECRL latch for the case that 'enable' signal is '1' only when input values are changed.

It is concluded from Figs. 5 and 6 that φ_2 would be better to power the input buffers when data are stored in the latch every cycle, and that φ_0 would be the best choice for the power supply clock for the input buffers otherwise.

4. A 16 × 8-bit shift register with a power supply clock generator

The energy consumption of the ECRL circuits should include that of the power supply clock generator for a fair comparison with the static CMOS circuits since the ECRL circuits require a power supply clock generator

Table 2
The energy consumption of each gate in ECRL latch for the case that 'enable' signal is '1' only when input values are changed

Energy consumption (pJ)	Phase of the power supply clock		
	φ_0	φ_2	φ_3
Total energy	0.160 (100%)	0.232 (100%)	0.178 (100%)
Input buffers I2, I3, I4	0.091 (56.9%)	0.003 (1.3%)	0.015 (8.4%)
NAND A1	0.008 (5%)	0.012 (5.2%)	0.011 (6.2%)
Switching MOS M1, M2	0.008 (5%)	0.124 (53.4%)	0.021 (11.8%)
Feedback buffer I1	0.053 (33.1%)	0.093 (40.1%)	0.131 (73.6%)

Enable = '1' only when the input signal is flipping.
Flipping period of input values: 20 ns.

for proper operation [8]. However, the energy consumption of a single latch with a power supply clock generator is meaningless since the energy consumption of a single latch is much smaller than that of a power supply clock generator, and only one power supply clock generator is necessary regardless of the size of a circuit. Therefore, the energy consumption of a 16×8-bit shift register file with a power supply clock generator is compared with that of the CMOS TSPCL shift registers with the same configuration.

Figs. 7 and 8 shows the schematic of the power supply clock generator and an 8-bit shift register, respectively [8,11]. If the latches are connected directly, the power supply clocks with the same phase are applied to the forward NAND gate of the current stage and the backward inverter of the next stage, which results in a short-circuit path. Therefore, the shift register would not work properly. It can be prevented by inserting a buffer between latches. Fig. 9 shows the simulated waveforms of an 8-bit ECRL shift register with the power supply clock generator. It shows the shift operation of the register for the input values.

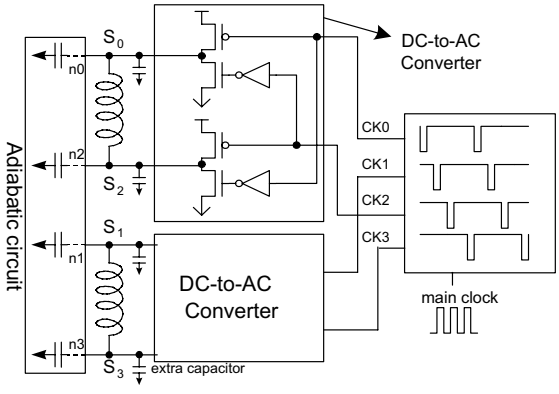

Fig. 7. The schematic of the power supply clock generator.

The energy consumption of a 16×8-bit shift register file includes that of the power supply clock generator. The efficiency of the power supply clock generator depends on the size of switching transistors which supply current to power supply clock nodes [8]. Table 3 shows optimal sizes of the switching NMOS transistors for the operation frequencies of 100, 200, 300 and 400 MHz. The size increases as the operation frequency increases since the power supply clock generator should supply more current as the operation frequency is increased. The sizes of PMOS transistors are doubled.

Fig. 10 shows the energy consumption of 16×8-bit ECRL shift registers with a power supply clock generator, 16×8-bit CMOS TSPCL shift registers, and the power supply clock generator only for various operation clock frequencies. The 'enable' signal is always '1' and input values are updated every 10 ns. The operation clock frequency does not affect the energy consumption of the CMOS circuits as expected, and the change of the energy consumption for ECRL circuits is also negligible though the energy consumption is decreased slightly. The ECRL circuit with the power supply clock generator consumes about 2/3 of the CMOS circuits. The energy consumption of the power supply clock generator is about 1/3 of that of the entire circuit. Fig. 10 also shows that the power supply clock generator supplies almost the same energy for various operation frequencies though the size of the switching transistors in the clock generator circuits is increased.

Fig. 11 shows the energy consumption of the shift registers when the flipping periods of input values are 10, 20, 40, and 80 ns, and when the 'enable' signal is always '1'. The operation clock frequency is 100 MHz. Both CMOS and ECRL circuits consume less energy as the input flipping period is increased. The energy

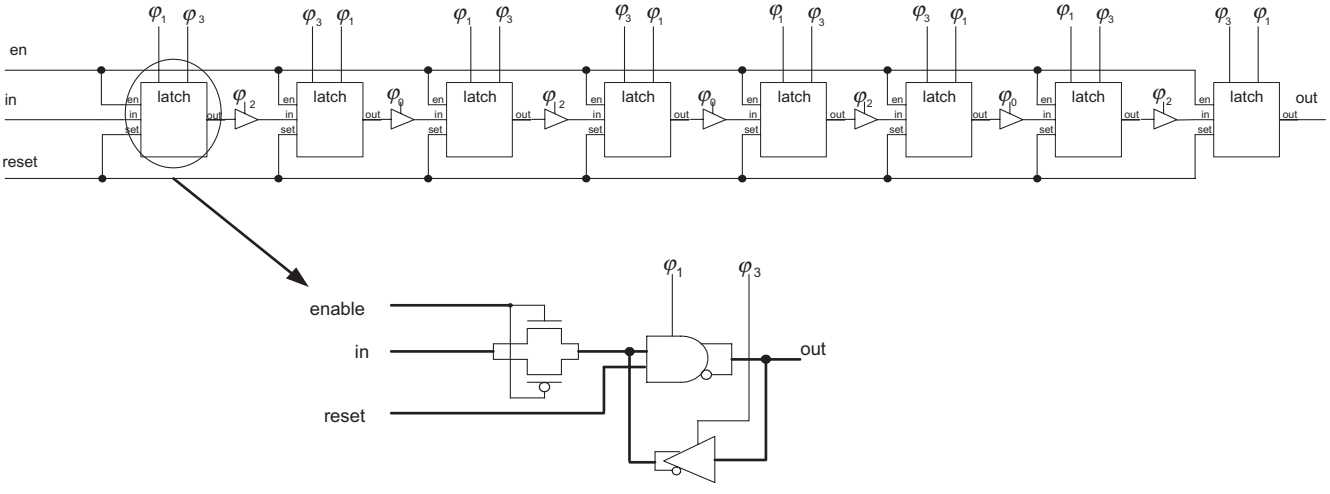

Fig. 8. The structure of a 16×8-bit shift register file.

Fig. 9. The SPICE simulation result of a 16×8-bit shift register file.

Table 3
The size of NMOS switching transistors of a power supply clock generator at an optimal energy efficiency

Operation frequency (MHz)	100	200	300	400
Width (μm)	7	18	30	40

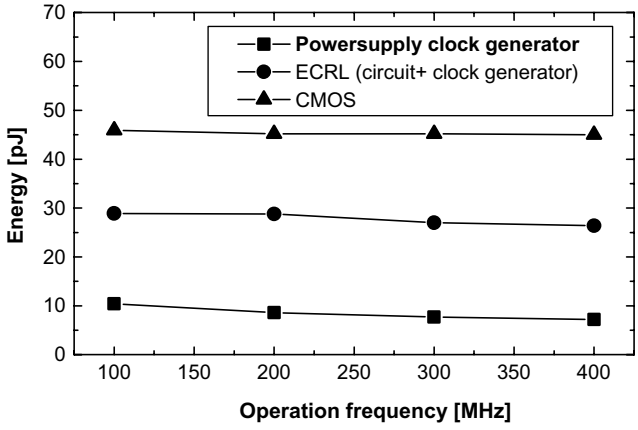

Fig. 10. The energy consumption of a 16×8-bit shift register file for the various supply clock frequencies.

consumption of ECRL registers is about 52.1–63.7% of that of CMOS registers, and that of the power supply clock does not change significantly. A number of combination logic gates and memory elements are included in practical circuits and only one power supply clock generator is necessary. Therefore, the energy consumption of the power supply clock generator is not significant in practical circuits, and the efficiency of energy consumption is increased. If a system is large enough, the energy consumption of ECRL circuits will be below 1/3 of that of CMOS circuits.

Fig. 12 shows the energy consumption of the shift registers for the case that the 'enable' signal is '1' for 10

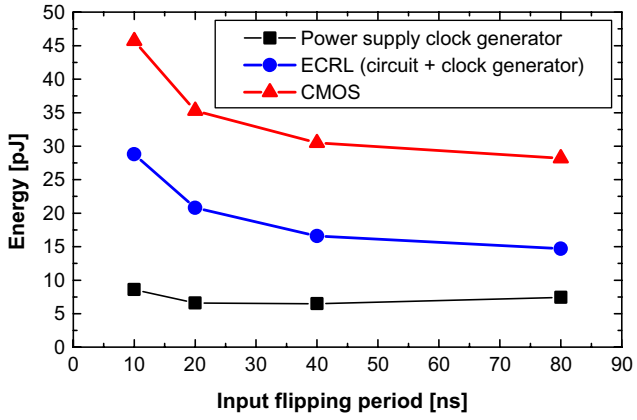

Fig. 11. The energy consumption of a 16×8-bit shift register file when 'enable' signal is always on.

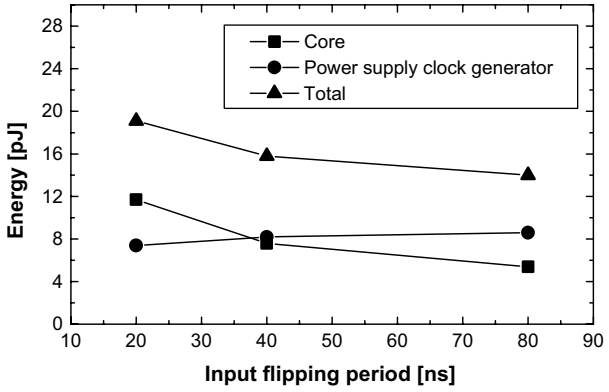

Fig. 12. The energy consumption of a 16×8-bit shift register file for the case that 'enable' signal is '1' only when input values are changed.

ns only when the input value changes. The energy consumption is decreased as the input flipping period is increased. However, it is decreased more slowly than that of a single latch since the input buffers driven by φ_0

and φ_2 are included together. The overall energy consumption is reduced by 10–15% compared with the case of the 'enable' signal is always '1'.

5. Conclusions

An ECRL latch for a storage element in low power adiabatic circuit is proposed and the characteristics are analyzed. The ECRL latch consists of a NAND gate, an inverter, and two MOSFET switches, and has the input signals of 'enable', 'reset', and 'input'. A single ECRL latch and a 16×8-bit shift register file with a power supply clock generators are designed, and the energy consumption is analyzed. The energy consumption is about half of a CMOS flip-flop and registers with the same configuration, and is expected to be 1/3 in practical circuits which include more combinational logic gates and memory elements. The energy consumption is not affected by the power supply clock frequency in the range of 100–400 MHz. The proposed ECRL latch can be a good choice of a low power storage element in adiabatic circuits.

Acknowledgements

This work was supported by the Soongsil University Research Fund.

References

[1] H. Lee, J. Kim, J. Korean Phys. Soc. 42 (2003) 255.
[2] Y.-W. Kim, H.S. Kang, C.-B. Oh, M.-H. Oh, S.-H. Yoo, B.-S. Kim, S. Park, K.-P. Suh, J. Korean Phys. Soc. 42 (2003) 206.
[3] J.S. Denker, IEEE Symp. on Low Power Electronics, October 10–12, 1994, p. 94.
[4] A. Kramer, J.S. Denker, S.C. Avery, A.G. Dickinson, T.R. Wik, Symp. on VLSI Circuits Dig. of Tech Papers, Honolulu, USA, June 9–11, 1994, p. 25.
[5] R.T. Hinman, M.F. Schlecht, Symp. on VLSI Circuits Dig. of Tech. Papers, Honolulu, USA, June 9–11, 1994, p. 19.
[6] A.G. Dickinson, J.S. Denker, IEEE J. Solid-State Circ. 30 (1995) 311.
[7] J. Lim, K. Kwon, S.-I. Chae, Electron. Lett. 34 (1998) 19.
[8] Y. Moon, D.K. Jeong, IEEE J. Solid-State Circ. 33 (1998) 696.
[9] Y. Moon, D.K. Jeong, IEEE J. Solid-State Circ. 31 (1996) 514.
[10] J.M. Rabaey, Digital Integrated Circuits, Prentice Hall, Englewood Cliffs, NJ, 1999, pp. 359–362.
[11] Y. Moon, J. IEEK SD 38 (4) (2001) 43.