

A stable U-band VCO in 65 nm CMOS with -0.11 dBm high output power

Jongsuk Lee and Yong Moon

Abstract — A high output power VCO (voltage controlled oscillator) in the U-band was implemented using a 65 nm CMOS process. The proposed VCO used a transmission line to increase output voltage swing and overcome the limitations of CMOS technologies. Two varactor banks were used for fine tuning with a 5% frequency tuning range. The proposed VCO showed small variation in output voltage and operated at 51.55-54.18 GHz. The measured phase noises were -51.53 dBc/Hz, -91.84 dBc/Hz, and -101.07 dBc/Hz at offset frequencies of 10 kHz, 1 MHz, and 10 MHz, respectively, with stable output power. The chip area, including the output buffer, is 0.16×0.16 mm² and the maximum output power was -0.11 dBm. The power consumption was 33.4 mW with a supply voltage of 1.2-V. The measured FOM_P was -190.8 dBc/Hz.

Index Terms—CMOS, voltage controlled oscillator (VCO), U-band, transformer, transmission line

I. INTRODUCTION

VCO is a necessary component when it comes to implementing a single-chip radio in a communication system [1-7]. However, CMOS VCOs have the limitation of a low quality factor (Q-factor) using on-chip passive components [1-8]. Thus, a transformer feedback technique is used to increase the output voltage swing, and the inductor of the LC oscillator based on transmission line theory enhances high frequency performance [2-3,6]. A high output power results in correct data transfer but deterioration of the phase noise performance. It is difficult to obtain high output power for the VCO operating at the U-band [1-3,8]. The VCO gain (K_{VCO}) is also important

factor in the VCO and a low K_{VCO} could improve the phase noise performance [7]. The change of the capacitance in the LC resonator determines the tuning range of the VCO, so the proposed VCO uses two varactor banks for the fine tuning range.

The remainder of this paper is organized as follows. In Section II, the proposed transformer VCO topology and circuit design are presented. The circuit implementation is described in Section III while post-simulation results and experimental results of the VCO are provided in Section IV. Finally, the conclusion is given in Section V.

II. VCO ARCHITECTURE AND CIRCUIT DESIGN

The architecture of the proposed VCO is an NMOS cross-coupled pair differential LC type and the transformer inductors are spiraled by L_{P1} , L_{P2} and L_{S1} , L_{S2} as shown in Fig. 1. The transformer inductors can provide drain-to-source feedback and voltage swing below ground level. The two varactor banks— C_{B1} and C_{B2} —are used to widen the tuning range of the VCO. The value of C_{VAR1} is twice that of C_{VAR3} .

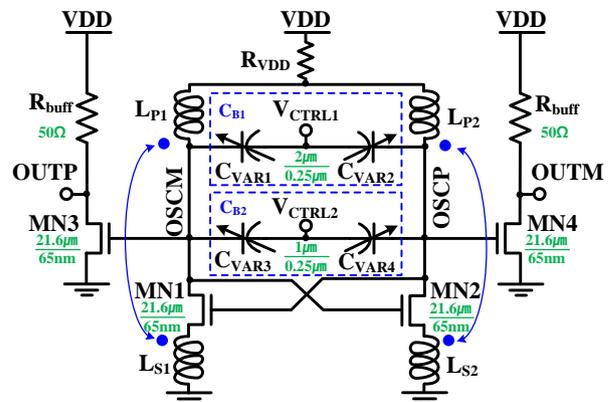


Fig. 1. Schematic of the proposed VCO

The resonant frequency of LC VCO is determined by the inductance, capacitance and parasitic resistance of an inductor and capacitor. R_{VDD} reduces output swing variation by preventing noise influx from the power supply to the VCO. In addition, R_{VDD} increases the resonant frequency because the capacitance of the varactor is decreased by lowering the DC voltage level of the varactor on the anode side—OSCM and OSCP. The output buffers, MN3 and MN4, are added to isolate the output of the VCO from other blocks but the output swing is reduced according to R_{buff} . If we use the inductor instead of the resistor, the output swing could increase and the power consumption could be reduced but the chip area will increase significantly. Moreover, the output buffer supports the 50Ω matching network.

The cross-coupled pair of MN1 and MN2 ensures the differential mode operation and compensates for the loss caused by the passive components. The size of MN1 and MN2 is selected to guarantee sufficient gain to maintain the oscillating condition and better phase noise performance. The negative resistance of the cross-coupled pair cancels out the positive resistance of the LC tank for oscillation. The NMOS core is suitable for operating at high frequency, because the current driving capability of NMOS is better than that of PMOS.

III. CIRCUIT IMPLEMENTATION

The designed VCO was implemented using a 65 nm CMOS process and verified by CADENCE Spectre RF simulator and measurement. In post-simulation, we used the PSN (Power Supply Network) model [9] to correctly predict the variation due to external supply in the measurement environment, as shown in Fig. 2.

When the PSN model was used, we could confirm that the variation of the VCO output swing was about 4.9 times larger than without the PSN model, as shown in Fig. 3. This means that the prediction of VCO operation using the PSN model was close to the measurement values.

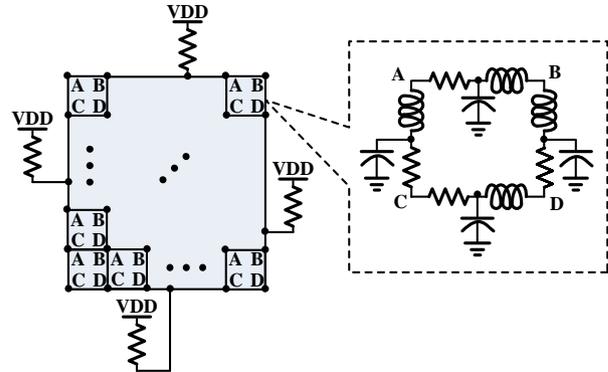


Fig. 2. The PSN model

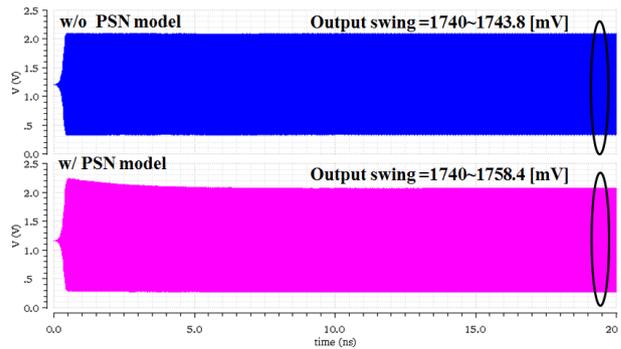


Fig. 3. Simulation results of the VCO output swing variation with and without the PSN model

We simulated the performance of the VCO considering the effect of external supply using the PSN model. We considered various operating conditions before implementation. The simulation results considering the R_{VDD} in PVT (Process, Supply voltage, and Temperature) variation are summarized in Table I and shown in Fig. 4. In these simulations, V_{CTRL1} and V_{CTRL2} were 0.6-V and the offset frequency of the phase noise simulation was 10MHz.

Table I. Simulation results for PVT variation using the PSN model

		w/o R_{VDD}			w/ R_{VDD}		
		Swing var. [mV]	Output freq. [GHz]	Phase Noise [dBc/Hz]	Swing var. [mV]	Output freq. [GHz]	Phase Noise [dBc/Hz]
Process	SS	2.43	50.611	-100.765	0.18	51.666	-96.669
	TT	6.12	51.314	-102.886	0.2	53.299	-100.436
	FF	11.46	52.127	-102.471	0.5	53.995	-100.61
Voltage [V]	1.08	4.74	51.698	-101.185	0.32	53.789	-98.158
	1.32	7.47	51.022	-104.153	0.16	52.883	-98.701
Temp. [°C]	0	9.09	51.41	-95.953	0.18	53.481	-101.565
	85	2.04	51.122	-100.893	0.42	52.687	-97.164

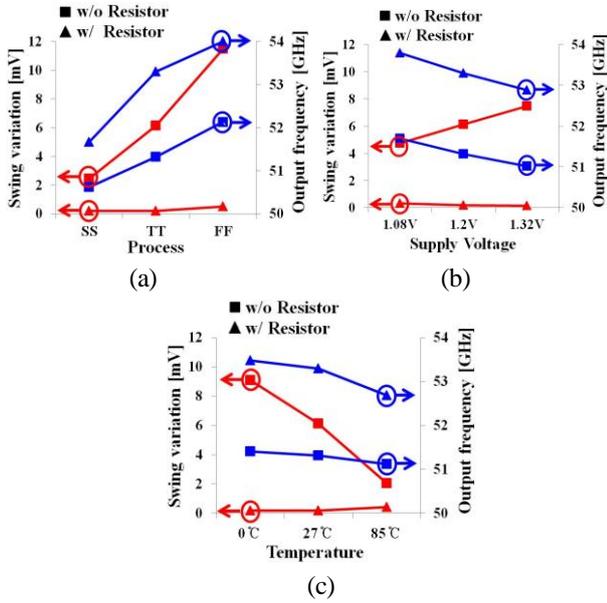


Fig. 4. Graph of the simulation results for (a)process variation (b)supply voltage variation (c)temperature variation

From the simulation results, the VCO including R_{VDD} showed small variation in output swing and operated at a higher frequency. The minimum output swing ratio was 4.9 times when the temperature was 85 °C, and the maximum ratio was 50.5 times when the temperature was 0°C. In phase noise performance analysis, R_{VDD} typically degenerates the performance because the noise of the R_{VDD} is added. However, in temperature simulation, when the variation of power supply is large, using the R_{VDD} show better phase noise characteristics. Therefore, if the power supply exhibits variation of DC voltage in the measurement, the R_{VDD} could improve the phase noise characteristics. As a result, we were able to determine that the VCO with R_{VDD} showed better performance in stability and that the operating frequency was increased about 4.1%. The drawback of using a resistor is that the inherent thermal noise of R_{VDD} worsens the phase noise characteristics, but the phase noise degeneration could be reduced to below 1 dBc/Hz if R_{VDD} were less than 10 Ω .

The VCO chip microphotograph is shown in Fig. 5. Eight pads were placed for probing. Four pads at the bottom side were used for GSSG probing, while the other pads for VDD, VSS, V_{CTRL1} , and V_{CTRL2} were placed on the other sides for DC biasing. The four inductors were implemented using a transmission line and L_{P1} (or L_{P2}) was placed close to L_{S1} (or L_{S2}) to obtain high mutual inductance. To determine the size of the inductor with

high Q-factor, we used an HFSS electromagnetic field simulator, Fig.6 show the simulation structures used to evaluate the proposed inductor.

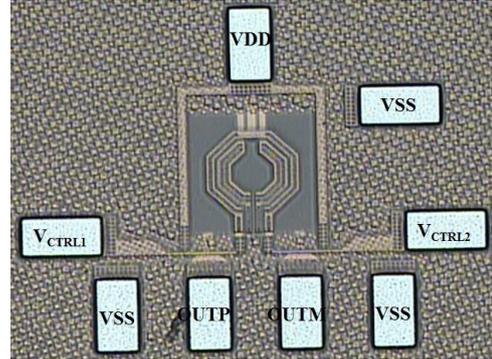


Fig. 5. VCO chip microphotograph

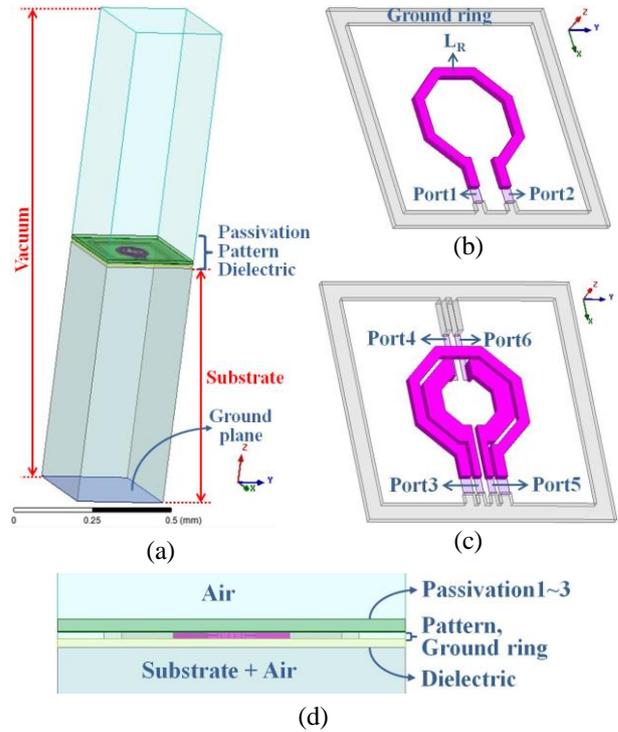


Fig. 6. 3-D Simulation structures of the proposed inductor (a)overall view (b)pattern for the simulation of L_{P1} and L_{P2} only (c)pattern for the simulation of all inductors (d)cross-section view

In Fig. 6(a), the thickness of the substrate and passivation are the same as the PDK parameter for process, and the vacuum plays a role in the radiation boundary. We used simulations to confirm the self-inductance (L_{self}) and mutual-inductance (M). The pattern used to obtain L_{self} is shown in Fig. 6(b) and the pattern considering the M is shown in Fig. 6(c). The L_{P1} and L_{P2} presented by L_R were

designed with a center-tapped structure connected with the VDD in the middle of the inductor and the inductance of L_R determined resonant frequency with the capacitance of the varactors. L_{S1} and L_{S2} have a semicircle shape and Port 4 and Port 6 are connected with ground in Fig. 1 . A simple unified form of the inductance of planar spirals is shown in Eq. (1)-(2) and Table II shows the geometric values of the proposed inductor [10]:

$$L \approx \frac{\mu_0 n^2 d_{avg} c_1}{2} \left[\ln\left(\frac{c_2}{\rho}\right) + c_3 \rho + c_4 \rho^2 \right] \quad (1)$$

$$\rho = \frac{d_{out} - d_{in}}{d_{out} + d_{in}} \quad (2)$$

Table II. Geometric values of the proposed inductor

Parameter	Type	Value
Width [μm]	L_{P1}, L_{P2}	9
	L_{S1}, L_{S2}	15
Thickness [μm]	$L_{P1}, L_{P2}, L_{S1}, L_{S2}$	5.6
Space [μm]	Between L_{P1}, L_{P2} and L_{S1}, L_{S2}	3
Outer length [μm]	L_{P1}, L_{P2}	100
	L_{S1}, L_{S2}	76
Calculated inductance [nH]	$L_R (=L_{P1} \text{ and } L_{P2})$	0.192

In Eq. (1)-(2), n is the number of turns, d_{avg} is the arithmetic mean of the inner and outer diameters, d_{out} is the outer diameter, d_{in} is the inner diameter, and ρ is the fill factor. Furthermore, c_1 - c_4 are the coefficients for the current-sheet inductance and they are shown in Table III [10]. Thus, the calculated inductance of L_R from Eq. (1) is 0.192 nH.

Table III. Coefficients for current-sheet inductance formula

Shape	c_1	c_2	c_3	c_4
Octagon	1.07	2.29	0	0.19

Figure 7 is the simulation result of Fig. 6(b) : we designed the operation frequency of the proposed VCO to be 53 GHz. In Fig. 7(a), the inductance of the designed inductor is 0.195 nH at 53 GHz, and this value is almost the same as the value calculated Eq. (1). Thus, we were able to verify the design of L_R .

The Q-factor of the inductor is one of the most important factors to affecting the performance of the VCO

[1-8], and is calculated from $[\text{Im}(Y_{11})/\text{Re}(Y_{11})]$ [8]. Figure 7(b) shows the simulation result of the Q-factor, but the maximum value is not evident at 53 GHz. Rather, the maximum Q-factor was 31.5 at 31 GHz, while the Q-factor of the target frequency was 26.3. This is because L_{S1} and L_{S2} were laid out on the inside of the L_{P1} and L_{P2} in the transformer structure, and then the Q-factor was changed by the electric field. Thus, we developed the second simulation to match the Q-factor and oscillation frequency as shown in Fig. 6(c). Figure 8 depicts the simulation result of Fig. 6(c), and shows that we could obtain the maximum Q-factor at the operating frequency via the several modifications in the structure. In Fig. 8(b), the Q-factor of L_R is 17.18 and the Q-factor of L_{S1} is 28.44. The Q-factor and inductance of L_{S2} were the same as those of L_{S1} .

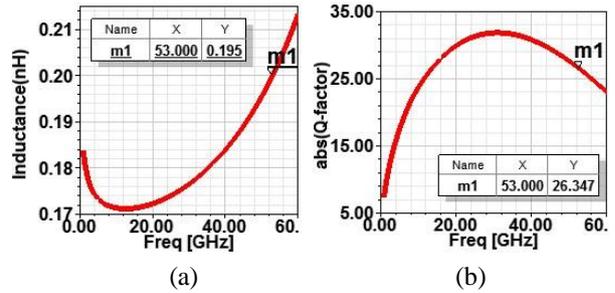


Fig. 7. HFSS simulation results of only the outside inductor (a)inductance of L_{P1}, L_{P2} (b)Q-factor of L_{P1}, L_{P2}

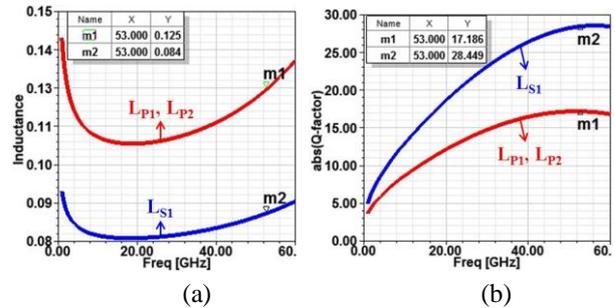


Fig. 8. HFSS simulation results of the inner and outside inductors (a)inductance of the L_{P1}, L_{P2} and L_{S1} (b)Q-factor of the L_{P1}, L_{P2} and L_{S1}

The inductance and capacitance of the proposed VCO to determine the oscillation frequency should be small due to the U-band operation. If the capacitance is too small, the operation range of the VCO will become narrow, so a design method that reduces the inductance is desirable. In the transformer structure, M is between two inductor, and the relationship between M and L_{self} is shown in Eq. (3)

[10]:

$$L_T = L_{self} \pm M \quad (3)$$

Here, L_T is the inductance of the L_R of Fig. 6(c), and M can be added and subtracted depending on the current direction flowing in the two inductors [10]. In the proposed structure, L_{P1} - L_{P2} and L_{S1} - L_{S2} are laid out as the current direction is reversed because the VCO can operate at high frequency if the inductance is reduced. From the simulation result, it was found that the inductance of L_R decreased from 0.195 nH to 0.125 nH (36%) : this is shown in Fig 8(a).

One of the important factors affecting the performance of VCO is the Q-factor of the varactor. In this paper, we focused on the analysis of the transformer inductor, so we used an NMOS structure in design. The corner simulation result of the Q-factor at 53 GHz versus V_{CTRL1} and V_{CTRL2} are shown Fig. 9. From the simulation result, we confirmed that the Q-factor value of the varactor used was less than the value of the previous modified varactor [5].

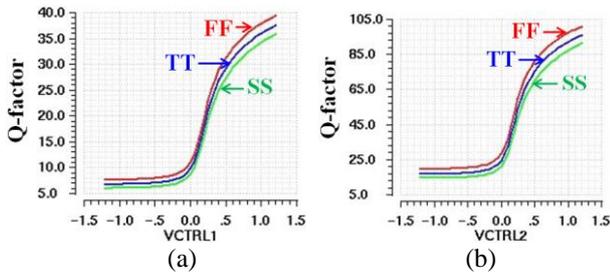


Fig. 9. PEX corner simulation results to the Q-factor of the C_{B1} and C_{B2} versus V_{CTRL1} and V_{CTRL2}

We were able to obtain the an advantage in terms of area via inductor coupling; the area of the proposed VCO including the output buffer was only $0.16 \times 0.16 \text{ mm}^2$. We optimized the width and length of the inductor to maximize the output power as much as possible. If coupling coefficient k is 1, the output swing can be calculated using Eq. (4) [6]. The source connected to the inductor could go below ground. If the value of inductor is too large, the oscillation is not maintained.

$$\text{Output swing} = \left(1 + \sqrt{\frac{L_P}{L_S}}\right) \cdot V_{DD} \quad (4)$$

IV. EXPERIMENTAL RESULTS

In the measurement, on-wafer probing was carried out using a probe station, N9010A spectrum analyzer, 11970V external mixer, N9029AE13 diplexer, and dual power supply. Figure 10 shows the experimental environment. The Infinity Probe could measure the output of the proposed VCO, while GSSG signifies ground-signal-signal-ground. The input of the mixer is a waveguide, so the adapter converts SMA to waveguide. The N9010A spectrum analyzer was able to measure the frequency upto 32 GHz but the diplexer changed the measurement frequency, so the U-band operation could be measured.

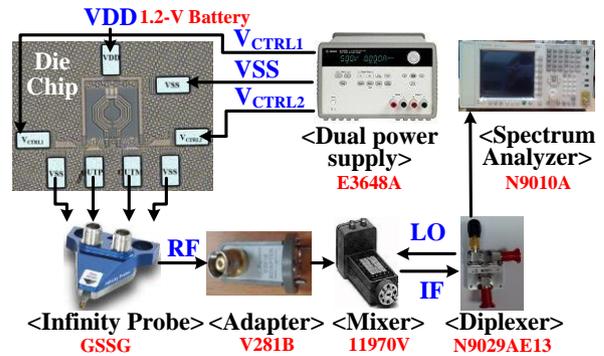


Fig. 10. The experimental environment of the proposed VCO

Figure 11 shows the measured frequency tuning range; the proposed VCO operated from 51.55 to 54.18 GHz. The capacitance of C_{B1} was greater than that of C_{B2} , so the tuning range from V_{CTRL1} was wider than from V_{CTRL2} . The reason for the narrowness of the operating range compared with previous works was that the capacitance of the VCO was small for fine tuning at the U-band [1-3]. The maximum K_{VCO} of the V_{CTRL1} was 1.52 GHz/V and the maximum K_{VCO} of the V_{CTRL2} was 0.67 GHz/V.

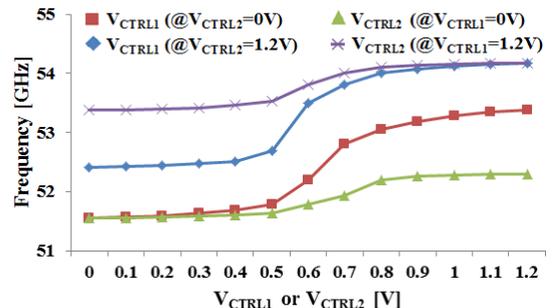


Fig. 11. The measured oscillating frequency of the VCO versus V_{CTRL1} and V_{CTRL2}

Figure 12 shows the power consumption, including the output buffer, in V_{CTRL1} and V_{CTRL2} ; the average value was 33.4 mW with a power supply of 1.2-V. The power consumption showed little change, but decreased even if the output frequency increased. The VCO core operated rapidly when the output frequency increased, so the power consumption of the VCO core also increased. On the other hand, the power consumption of the output buffer decreased due to the decrease in the output swing. The reason for the high power consumption compared with the previous works is that the output buffer had a 50Ω resistor for impedance matching between OUTP or OUTM and the cable dissipated a large amount of power.

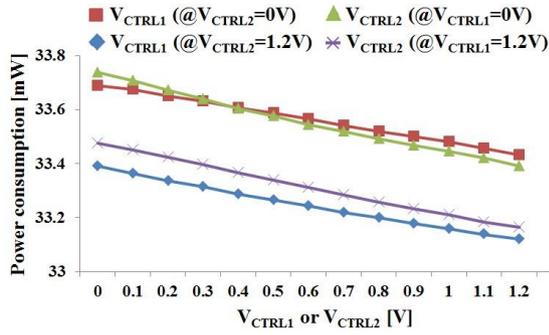


Fig. 12. The measured power consumption of the VCO versus V_{CTRL1} and V_{CTRL2}

The measured output power was -14.96 dBm when V_{CTRL1} and V_{CTRL2} were 1-V as shown in Fig. 13.

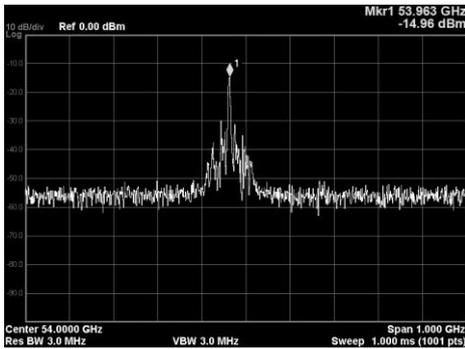


Fig. 13. Measured spectrum of the VCO

Losses were evident in the measurement environment, and it is shown in Table IV, which incorporates information from datasheets. We compensated the losses of the probe, adapter, cable (three 5061-5458 cable and one 124-605 cable), and diplexer from the measured output power. The loss of the mixer was automatically compensated for by a spectrum analyzer according to the

frequency. Finally, the compensated output power was -0.11 dBm, representing a very large value in the millimeter wave data transfer system.

Table IV. Loss table of the measuring equipment

Product name	Model name	Type	Loss [dB]
Probe	Infinity	Insertion loss	1.2
Adapter	V281B	Insertion loss	0.5
Mixer	11970V	Conversion loss	34.2~35.6 (Auto tune)
Cable	5061-5458	Insertion loss @6GHz	1.1
	124-605	Insertion loss @67GHz	6.85
Diplexer	N9029AE13	IF Insertion loss	1.5
		LO Insertion loss	1.5

The measured phase noises were -51.53 dBc/Hz, -91.84 dBc/Hz, and -101.07 dBc/Hz at offset frequencies of 10 kHz, 1 MHz, and 10 MHz, respectively, when the VCO was operating at 51.672 GHz (Fig. 14).



Fig. 14. Measured phase noise versus offset frequency

The proposed VCO was compared to other works to verify its performance by using measured values. FOM_P was used for the evaluation and is defined in Eq. (5) [8]:

$$FOM_P = L(\Delta f) - 20 \log\left(\frac{f_0}{\Delta f}\right) - \log\left(\frac{P_{RF}}{1mW}\right) - 10 \log(\eta) \quad (5)$$

Here, $L(\Delta f)$ is the phase noise, Δf is the offset frequency, f_0 is the oscillation frequency, P_{RF} is the RF output power, and η is the dc-to-RF efficiency, defined as:

$$\eta = \frac{P_{RF}}{P_{DC}} \times 100\% \quad (6)$$

In Eq. (6), P_{DC} is the DC power consumption. The proposed VCO showed superior performance compared with existing VCO's using the same process technologies. Table V summarizes the performance comparison between the proposed work and recently reported works.

Table V. Performance summary and comparisons

	[1]JSSC 2015	[2]TMTT 2015	[3]TCSI 2014	This work
Process	32 nm SOI CMOS	65 nm CMOS	65 nm CMOS	65 nm CMOS
Operating frequency [GHz]	46.4~58.1	47.6~71	57~65.5	51.55~54.18
Phase noise [dBc/Hz]	-89@1MHz	-101~113 @10MHz	-110@10MHz	-51.53@10kHz -91.84@1MHz -101.07@10MHz
Output power [dBm]	-7~0	-14~16	-20.97	-0.11
Area [mm ²]	0.049	0.074	*0.141	*0.025
P_{DC} [mW]	11.45	8.9~10.4	6	*33.4
FOM _p [dBc/Hz]	-182.7	-166	-157	-190.8
Supply [V]	0.55	1	1	1.2

*Including output buffer area

V. CONCLUSIONS

A stable VCO in the U-band using a 65 nm CMOS with high output power and excellent FOM_p was designed in this work. The VCO topology was the NMOS cross-coupled pair differential LC type using a transmission line and a drain-to-source feedback structure for high output swing. A resistor was added to the VCO to obtain stable output swing. The inductors are located close to each other to obtain a high Q-factor and large inductance. This structure has an advantage in area, and the area of proposed VCO was 0.16×0.16 mm². Two varactor banks were used to widen the tuning range and the measured operating frequency range was from 51.55 to 54.18 GHz. The measured output power was -0.11 dBm and the phase noises were -51.53 dBc/Hz, -91.84 dBc/Hz, and -101.07 dBc/Hz at offset frequency of 10 kHz, 1 MHz, and 10 MHz, respectively. The power consumption was 33.4 mW with a power supply of 1.2-V and the FOM_p was -190.8 dBc/Hz, which showed better performance than previous works.

In this research, the proposed VCO was found to be feasible for application in millimeter wave data transfer systems and so on.

CAD tool and MPW were supported by IDEC.

ACKNOWLEDGMENTS

This work was partly supported by the IT R&D program of MOTIE/ KEIT. [10044092, Development of Core IPs of OFDM PHY and RF Transceiver for 60GHz Wireless LAN/PAN in application of 7Gbps Wireless Multimedia Services] and also supported by the Human Resources Development program (No.20144030200600) of the Korea Institute of Energy Technology Evaluation and Planning (KETEP) grant funded by the Korea government Ministry of Trade, Industry and Energy.

REFERENCES

- [1] Bodhisatwa Sadhu, Mark Ferriss, and Alberto Valdes-Garcia, "A 52 GHz Frequency Synthesizer Featuring a 2nd Harmonic Extraction Technique That Preserves VCO Performance," *IEEE, J. Solid-State Circuits (JSSC)*, Vol.50, No.5, pp.1214-1223, May, 2015.
- [2] Haikun Jia, Baoyong Chi, Lixue Kuang, and Zhihua Wang, "A 47.6–71.0-GHz 65-nm CMOS VCO Based on Magnetically Coupled -Type LC Network," *IEEE, Transactions on Microwave Theory and Techniques (TMTT)*, Vol.63, No.5, pp.1645-1657, May, 2015.
- [3] Wei Fei, HaoYu, Haipeng Fu, Junyan Ren, and Kiat Seng Yeo, "Design and Analysis of Wide Frequency-Tuning-Range CMOS 60 GHz VCO by Switching Inductor Loaded Transformer," *Circuit and Systems I: regular papers, IEEE Transactions on (TCSI)*, vol. 61, no. 3, pp. 699-711, 2014.
- [4] Namhyung Kim, Jongwon Yun, and Jae-Sung Rieh, "A 120 GHz Voltage Controlled Oscillator Integrated with 1/128 Frequency Divider Chain in 65 nm CMOS Technology" *J. Semiconductor Technology Science*, Vol.14, No.1, pp.131-137, Feb. 2014.
- [5] Changhua Cao and Kenneth K.O., "Millimeter-wave voltage-controlled oscillators in 0.13- μ m MOS

technology,” IEEE, J. Solid-State Circuits (JSSC), Vol.41, No.6, pp.1297-1304, Jun. 2006.

- [6] Yu-Hsuan Lin, Jeng-Han Tsai, Yen-Hung Kuo, and Tian-Wei Huang, “An ultra low-power 24 GHz Phase-lock-loop with low phase-noise VCO embedded in 0.18 μm CMOS process,” IEEE, Asia-Pacific Microwave Conference Proceedings (APMC), pp.1630-1633, Dec. 2011.
- [7] R. M. Weng and J. Y. Lin, “A 2.4 GHz Low Phase Noise Voltage Controlled Oscillator,” Proceedings of Progress in Electromagnetics Research Symposium, pp. 546-550, Mar. 2009.
- [8] Che-Chen Lee, Shu-Yan Huang, and Hong-Yeh Chang, “A 44-49 GHz Low Phase Noise CMOS Voltage-Controlled Oscillator with 10-dBm Output Power and 16.1 % Efficiency,” Microwave Symposium (IMS), 2014 IEEE MTT-S International, pp. 1-4, Jun. 2014.
- [9] Chang-Ryong Heo and Chong-Suck Rim, “Decoupling Capacitance Allocation Noise Reduction,” Journal of The Institute of Electronics Engineers of Korea, Vol.42, No.9, pp.270-276, Sep. 2005.
- [10] Thomas. H. Lee, “The Design of CMOS Radio-Frequency Integrated Circuits,” CAMBRIDGE, U.k. : CAMBRIDGE Univ. Press, pp.136, 2004.



Jongsuk Lee was born in Seoul, Korea, in 1981. He received the B.S. degree in the School of Electronic Engineering from Soongsil University, Korea, in 2009. He is currently pursuing the Ph.D. degree in the Department of Electronic Engineering from Soongsil University. His research interests include analog PLL and all digital PLL.



Yong Moon received the B.S., M.S., and Ph.D. degrees from the Department of Electronics Engineering, Seoul National University, Seoul, Korea, in 1990, 1992 and 1997, respectively. From 1997 to 1999, he was with LG Semicon co., Ltd., where he contributed to senior research engineer. Since 1999, he has been with Soongsil University, Seoul, Korea, where he is a professor with School of Electronic Engineering. His research interests include PLL, low-power circuit, mixed signal IC and RF circuits.